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Concatenated Reed-Solomon Inner and Convolutional Outer Codes for Mobile Channels with Soft Core Processor Implementation

Usana Tuntoolavest*, Vasin Suktalordcheep and Jatupon Thonchai

ABSTRACT

The use of Reed-Solomon inner code in the Forney's concatenated code structure was proposed to correct longer burst errors in high speed mobile communications without interleaving. Vector Symbol Decoding (VSD) was selected as the outer code decoding of the large sized outer symbols (greater than 100 bits per symbol). The complete concatenated coding system with VSD was analyzed for both Bose-Chaudhuri-Hocquenghem (BCH) and Reed-Solomon (RS) inner codes. The inner decoder for BCH was a combined list and soft Viterbi algorithm (VA) or a soft VA, while the inner decoder for RS was an algebraic decoder. Results were shown for the BCH inner only, the VSD only and for the complete system. In a Rician channel with a carrier frequency of 2.1 GHz at 80 $km.hr^{-1}$ and a signal to noise ratio of 11 dB, the probability of decoding failure for the system with RS and hard decision was three magnitudes lower than the one with BCH and soft VA. For VSD only with no inner code, the larger sized symbols provided better performance in a burst error channel, while a smaller size was better in a random error channel. In addition, all the coding processes were implemented on a soft processor TSK 3000A and field programmable gate array boards to show that it was practical in terms of complexity.

Keywords: Vector Symbol Decoding, Reed-Solomon inner code, convolutional outer code, coding for mobile channels

INTRODUCTION

The concatenated codes proposed by Forney are practical, good, long codes, constructed simply from shorter codes (Forney, 1966). This structure was later called "serial concatenation" (Barg and Zémor, 2005) after other types had been developed, especially the "parallel concatenation" which included the turbo codes (Berrou *et al.*, 1993). A simple serial concatenated code has only a binary inner and a nonbinary outer code. Reed-Solomon (RS) codes are widely used outer codes due to their maximum distance properties and the ease of the design process from their guaranteed correction capabilities. The RS code is also one of the standard codes for space communication (Consultative Committee for Space Data Systems, 2012). The concatenated decoder consists of an inner decoder and an outer decoder. A Viterbi Algorithm (VA) is the optimal decoder for a convolutional inner code. For Bose-Chaudhuri-Hocquenghem (BCH) and RS codes, there are several possible decoders.

Nonbinary convolutional codes over a Galois field (GF) with especially large q, are not generally selected as the outer codes due to the impracticality of decoding them by the maximum likelihood decoder since the number

Department of Electrical Engineering, Faculty of Engineering, Kasetsart University, Bangkok 10900, Thailand.
* Corresponding author, e-mail: fengunt@ku.ac.th

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of computations is increased exponentially with q (Lin and Costello, 2004). In 2002, this problem was solved with Vector Symbol Decoding (VSD) that could decode any nonbinary convolutional codes with a large symbol size (Tuntoolavest and Metzner, 2002). In 2011, a "generalized concatenated coding system" was presented (Tuntoolavest *et al.*, 2011). Any combination of block and convolutional inner and outer codes was allowed with LVA-VSD (List Viterbi Algorithm-Vector Symbol Decoding) in Tuntoolavest and Noradee (2010). LVA was first proposed as the combined list and soft decoding for convolutional codes (Seshadri and Sundberg, 1994). The list inner decoding was chosen since it improved VSD performance. The list soft decoding for block inner code was proposed with the performance for an additive white Gaussian noise (AWGN) channel (Tuntoolavest *et al.*, 2011) and for fading channels (Thongchai *et al.*, 2013). Chana *et al.* (2011) presented a soft decoding for binary cyclic codes using the cyclic property, not the VA or the list decoding.

In this paper, the use of nonbinary inner codes is proposed, such as RS codes with a VSD outer decoder. This increases the symbol size manifoldly. The advantage of using larger sized symbols is that it can correct longer burst errors that result from the higher data rate required by the current and upcoming wireless communication standards. The proposed coding system can use any block or convolutional codes as the outer codes since they can be decoded with VSD. This paper focuses on the convolutional outer codes because their complexity is lower, especially when the channel is good. Reed-Solomon as the inner coding scheme was mentioned in Andreadou and Pavlidou (2010). However, it was not the concatenated code in Forney's structure as proposed in this paper. Their work was rather a cascading of a low-density parity-check outer code with an RS inner code for the power-line-communication channel (Andreadou and Pavlidou, 2010). In this paper, the complete nonbinary concatenated system is presented using both simulation and a hardware implementation. The VSD program was also modified to accept any symbol size up to 128 bits to allow BCH and RS inner codes in addition to the convolutional inner code in previous work. Specifically, implementation involved the outer convolutional, the inner BCH and RS encoders, the List-of 2 VA, the RS algebraic inner decoders and the VSD outer decoder.

In previous work, some functions have been implemented with VHDL (a very high speed integrated circuit hardware description language) such as an outer encoder (Tuntoolavest and Thonchai, 2011), the LVA for an inner convolutional code (Tuntoolavest and Noradee, 2010) and the pre-decoding of VSD (Tuntoolavest *et al.*, 2007) but not the main VSD functions. In this work, all programs were rewritten in the software programming language C instead of VHDL and the soft core processor was used for flexibility in testing many different conditions with the main objective to prove this new idea.

BACKGROUND

While this research requires some background in basic coding techniques such as RS codes, BCH codes, convolutional codes, concatenated codes, list decoding and soft Viterbi decoding, this information has been omitted due to limited space. Thus, this background covers notes on the concept of using nonbinary codes, the VSD technique to decode large nonbinary codes and list soft decoding for block inner codes to provide alternative choices for a VSD outer decoder. Many of these topics are based on the results from previous work and more details can be found in the cited references.

Nonbinary codes

Nonbinary codes are codes with symbols from GF(q) with $q > 2$. Most uses involve $q = 2^m$ where m is an integer to produce m-bit symbols. These codes are attractive in mobile channels

because they can correct burst errors directly without the delay caused by the interleaver. The nonbinary encoder is similar to that of the binary codes with some modifications on memory and the modulo-2 operation, as well as multiplication by the field elements. For example, a nonbinary RS encoder uses the shift register circuit to encode in a similar way to the BCH encoder with some modification as described in Lin and Costello (2004). The nonbinary convolutional encoder was described in detail in Tuntoolavest and Intharasakul (2006).

The nonbinary decoder is more complex than the encoder and so it is much more difficult to decode a nonbianry code than a binary one. For RS algebraic decoding, the error values must also be found in addition to the error positions. For VA, the computation increases exponentially with the size of the symbols. Examples of RS decoders are algebraic decoding using the Berlekamp–Massey approach (Lin and Costello, 2004), soft decision decoding (Koetter and Vardy, 2003) and iterative soft-decision decoding (Xia and Cruz, 2007). Because of their decoder complexity, nonbinary convolutional codes are not commonly used.

Vector symbol decoding

The principle of vector symbol decoding (VSD) was proposed in 1990 (Metzner and Kapturowski, 1990). It is a decoding technique for any linear nonbinary codes over GF(q) with large q. VSD has been applied for block codes (Oh and Metzner, 1994) and convolutional codes (Tuntoolavest and Metzner, 2002). The typical codes used 32-bit or at least 24-bit symbols (Tuntoolavest, 2004). This makes VSD different from other nonbinary decoders, which usually utilize small symbols. Even if VSD involves suboptimal decoding, it is flexible in terms of symbol size and easy to use. The detailed VSD decoding steps have been explained for convolutional codes (Tuntoolavest, 2009) and for block codes (Vanichchanunt *et al.*, 2009), where both studies used the same principle with some modifications. An interesting feature is that VSD decodes with the same steps regardless of the symbol size. For two received sequences that are erroneous in all the same positions, the ability of VSD to correct them is exactly the same; that is, the performance does not deteriorate with an increase in the symbol size (Tuntoolavest, 2009). This fact makes the design of the concatenated code with VSD very flexible and allows various types and length of inner codes.

Vector symbol decoding with alternative choices

One interesting feature of VSD is that the choices from the list inner decoder can improve the performance and reduce the decoding complexity as VSD also allows great flexibility regarding the number of choices from the list inner decoder as demonstrated by Tuntoolavest and Seubnaung (2007) whereby options allow symbols to have no choice, have one choice or have multiple choices. Tuntoolavest and Seubnaung (2007) concluded that the List-of-2 VA was most suitable from an implementation perspective.

Concatenated coding systems with vector symbol outer decoder

A concatenated coding system that uses VSD as the outer decoder is very flexible regarding the inner and the outer code selection (Thonchai, *et al.*, 2013). This paper focuses on the inner and outer codes as shown in Figure 1 since they are the new setups. The discussion and performance of VSD for block codes were presented in Metzner (2003) and for inner and outer convolutional codes in Tuntoolavest and Metzner (2002).

METHOD

The work was divided into two parts: the simulations and the soft core processor implementation. The first part involved the new concept and the simulations of the complete system with the Matlab (R2011b; MathWorks; Natick,

MA, U.S.A) and the C++ (Microsoft Visual Studio 2010; Microsoft; Redmond, WA, USA) programs. The second part mainly provided the proof of the concept. The hardware implementation for both the encoder and the decoder was done on the soft core TSK 300A processor (Altium Ltd.; Belrose, New South Wales, Australia) and FPGA (field programmable gate array) boards, using the Nanoboard3000.

Simulations

Two main concatenated coding systems were simulated; both used nonbinary (3,2,2) convolutional outer codes and were decoded with VSD. The first one used a BCH (31,26) binary block inner code and the second one used an RS (63,51) nonbinary block inner code. For the first system, two different outer symbol sizes were considered. The 26-bit outer symbol case used List-of-2 soft VA as the inner decoder. The 104-bit outer symbol case used soft VA with no list decoding as the inner decoder. For the second system, the inner decoder was an algebraic RS decoder. The channels under consideration were a two-state fading channel and the Rayleigh and the Rician fading channels with and without the Doppler Effect.

System I with a bose-chaudhuri-hocquenghem inner code: 26-bit and 104-bit outer symbols

In Figure 2, the inner code was the binary Bose, Chaudhuri and Hocquenghem (BCH) code

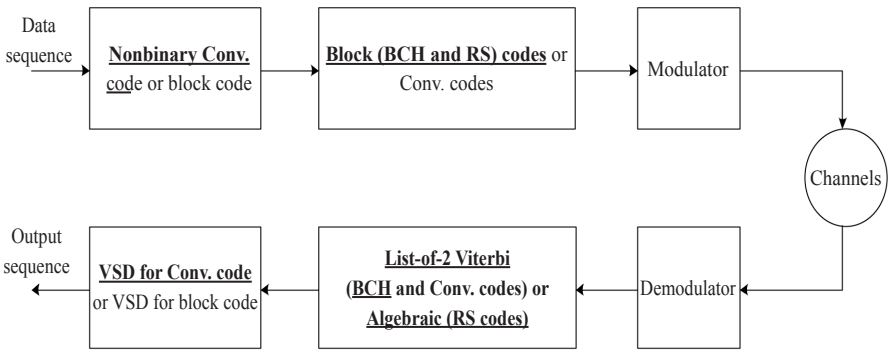

Figure 1 Block diagram of the concatenated coding system. Vector symbol decoding (VSD) outer decoders for various inner and outer codes are shown in bold underline. (BCH = Bose-Chaudhuri-Hocquenghem, RS = Reed-Solomon, Conv. = Convolutional.)

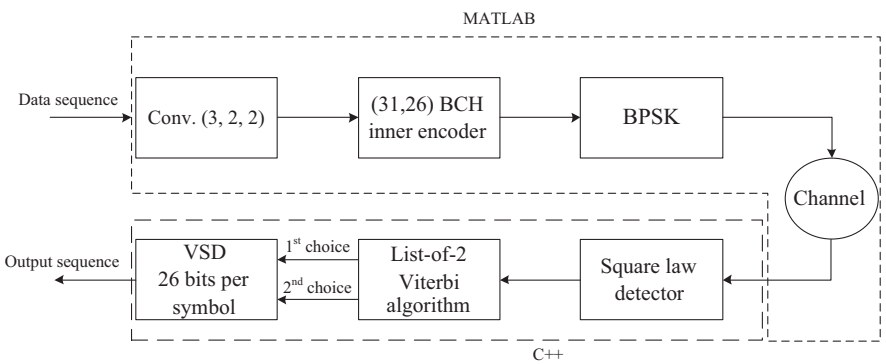

Figure 2 Block diagram for the inner Bose-Chaudhuri-Hocquenghem (BCH) case: 26-bit outer symbol case using the Matlab and C++ software programs. (VSD = Vector symbol decoding, BPSK = binary phase shift keying.)

of size (31,26). The outer code was the (3,2,2) convolutional code over a Galois field (GF) of (2^{26}) with the generator matrix in the transformed domain G(D) in Equation 1:

$$G(D) = \begin{bmatrix} 1+D+D^2 & D^2 & 1 \\ D & 1+D^2 & 1+D+D^2 \end{bmatrix} \quad (1)$$

The inner decoder was the List-of-2 soft VA. Two different sizes of outer symbols were analyzed. The first one was the 26-bit outer symbols as shown in Figure 2. The second one was the 104-bit outer symbols, where four inner symbols are grouped to one outer symbol as illustrated in Figure 3. For the 104-bit symbol, the soft Viterbi with no list was selected for the comparison with the RS decoder.

System II with a reed-solomon inner code: 102-bit outer symbols

This case is shown in Figure 1. The outer code is the (3,2,2) convolutional code and the inner code is the (63,51) RS code over GF(2^6). Each group of three outer symbols was considered as one inner input sequence of 51 symbols each of size 6-bits as shown in Figure 4. Each outer symbol was a 102-bit symbol. This was close to the 104-bit outer symbols in System I and was selected for the comparison between BCH and RS inner codes. For simulations, the outer code was a terminated convolutional code with 21 encoded symbols. However, the length of the outer code can be longer because a convolutional code can be terminated as desired. However, the decoding failure probability will increase with the length of the terminated convolutional code as explained in Tuntoolavest and Chaiwan (2012).

Mobile channels

The mobile channels under consideration were the Rayleigh fading channel, the Rician fading channel and the 2-state fading channel models. All channel models included the Doppler Effect resulting from the mobility of the transceivers. The 2-state fading model consisted of the fade state and the non-fade state. This model was used to generate burst errors. The main parameters were as shown in Equations 2–4 (Linnartz, 1993):

$$\text{Average fade duration (seconds)} = \frac{\sqrt{\eta}}{\sqrt{2\pi}\cdot f_d} \quad (2)$$

Average non-fade duration (seconds) =

$$\frac{\sqrt{\eta}}{\sqrt{2\pi}\cdot f_d}\cdot\left[e^{\left(\frac{1}{\eta}\right)} - 1\right] \quad (3)$$

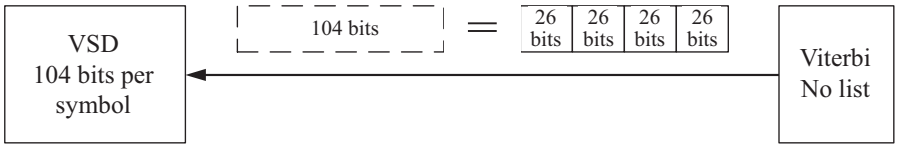

Figure 3 Decoder for the inner (31, 26) Bose-Chaudhuri-Hocquenghem (BCH): the 104-bit outer symbol case. (VSD = Vector symbol decoding.)

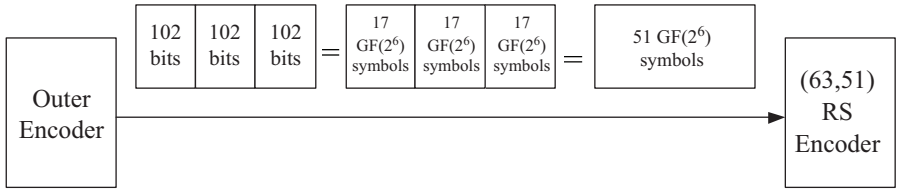

Figure 4 The encoder for the inner (63,51) Reed-Solomon (RS) code with 102-bit outer symbols. (GF = Galois field.)

$$\text{Crossing rate (per second)} = \frac{\sqrt{2\pi}\cdot f_d}{\sqrt{\eta}}\cdot e^{-\frac{1}{\eta}} \quad (4)$$

where η is the fade margin (the ratio of the local-mean signal power and the minimum power needed for reliable communications) and f_d is the Doppler spread given by Equation 5:

$$f_d = f_c \frac{v\cdot\cos(\gamma)}{c_0} \quad (5)$$

where f_c is the carrier frequency measured in Hertz, v is the velocity in meters per second that the receiver moves away from the transmitter, c_o is the speed of light = 3×10^8 m.s^{-1} and γ is the angle between the transmitter and the receiver.

System implementation

In the FPGA architecture shown in Figure 5, the soft processor TSK 3000A was used to control all interface devices associated with memory devices and the input/output parts. The input/output parts consisted of the Ethernet port for data transmission with a computer, the soft terminal for output display and the RS-232 port for data transmission using a wireless transceiver. The memory consisted of independent static memory and static memory, both configured to 1 Megabyte in size. For the Ethernet port in the FPGA device, the MAC address (02:34:45:56:67:78), the IP address of the FPGA (192.168.1.1) and the subnet mask (255.255.255.0) were set. The data source was also set in the same Local Area Network (LAN) with the IP address 192.168.1.2 and the same subnet mask as the FPGA. The data received or transmitted via the Ethernet port were buffered in the independent static memory. For the RS-232 port, the baud rate was set to 9,600 baud.s^{-1}. Asynchronous transmission was employed where each word consisted of 8 data bits, 1 start and 1 stop bit with no parity bit.

To connect Matlab with the FGPA hardware, the "Instrument Control Toolbox" from Matlab was used to transfer data over the Transmission Control Protocol/Internet Protocol (TCP/IP) packet. First, the TCP/IP object was created with the tcpip() function. Then, the data were transferred by the fwrite() function to the port and an IP address was created in the initialized step. In the FPGA board, the LWIP (Lightweight IP) was built. This is an open source TCP/IP networking stack for embedded systems; it manages the function of the TCP/IP packet. The fread() function was used to collected data from the FPGA. The real hardware used in this system is shown in Figure 6.

RESULTS

Figure 7 shows the decoding error probability (P_e) for the (31, 26) BCH inner code under several channel conditions. The list soft VA is simulated with the written C++ program. Each result was from 100,000 iterations. It can be noted that although the list soft VA provides two

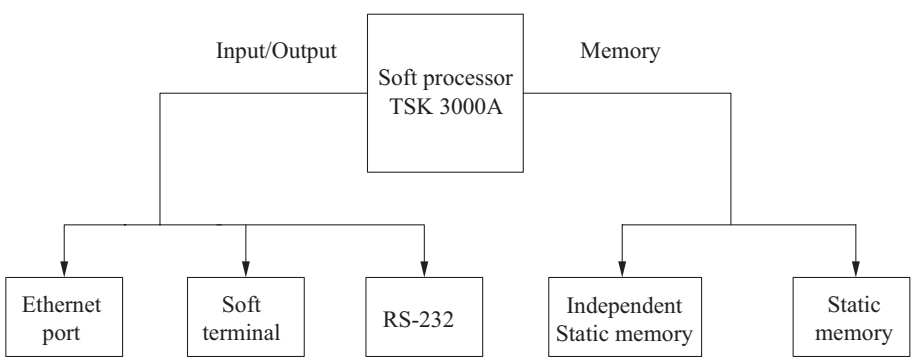

Figure 5 System architecture in the field programmable gate array.

choices, only the performance of the first choice is shown. Thus, these results are the same for the list soft and the soft VA. Differences will occur when the outer code is included. As expected, the hard VA was worse than the soft VA. The best channel was AWGN since a BCH code is a random error correcting code and this channel caused random errors, while the Rayleigh and Rician channels caused burst errors. For the soft VA, P_e was substantially lower when there was no Doppler effect. In addition, the value of P_e was approximately the same when the Doppler frequency (f_d) was changed from 155.54 Hz to 233.31 Hz. These values corresponded to the 2.1 GHz carrier frequency and velocities of 80 km.hr^{-1} and 120 km.hr^{-1}, respectively. The performance of the RS algebraic decoder was omitted due to limited space since it is widely known.

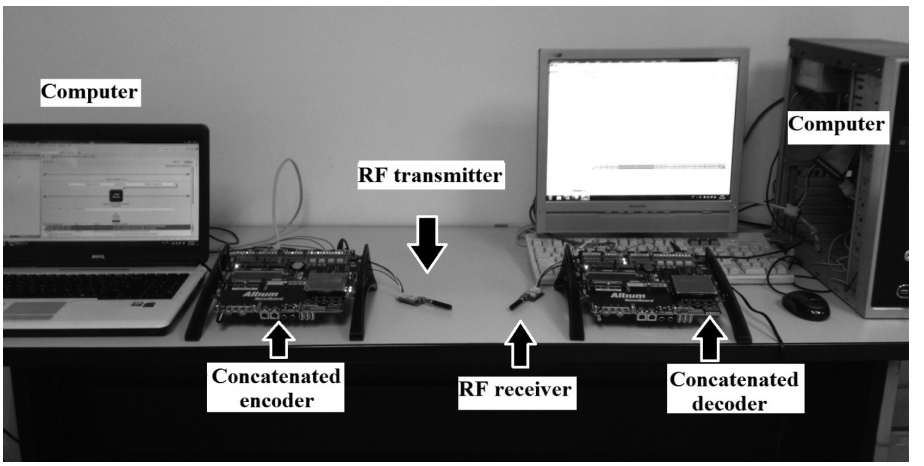

Figure 6 Actual hardware components for the radio frequency (RF) transmitter and receiver.

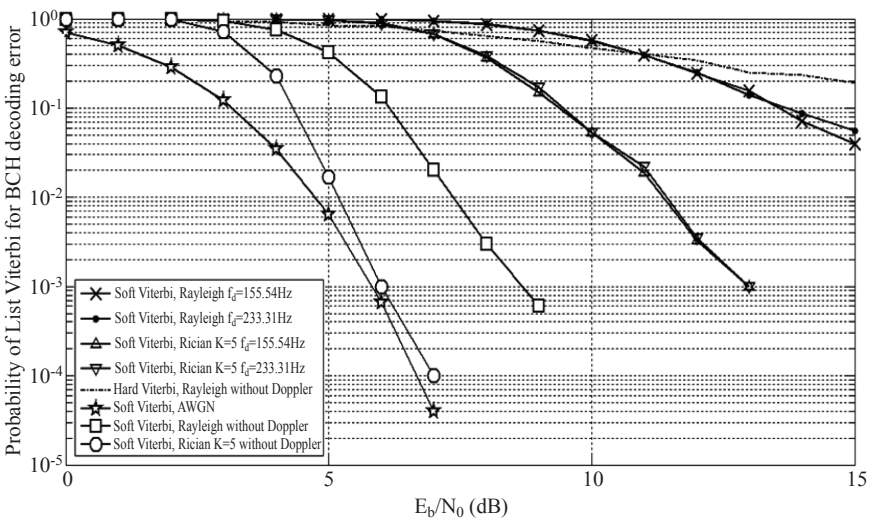

Figure 7 Performance of list soft and hard Viterbi algorithms for the (31, 26) Bose-Chaudhuri-Hocquenghem (BCH) code. (f_d = Doppler spread, AWGN = additive white Gaussian noise, E_b = energy per bit, N_0 = noise spectral density, K = Rician K-factor, which is the ratio of signal power in the dominant component to the scattered power.

Next, the outer decoder was considered without the inner coding system in order to understand the effect of using a different symbol size in the random error and burst error channels. The results in Figure 8 show that the smaller symbol size was better for the AWGN channel, which is representative of random error channels. The reverse was true for the 2-state channel model, which is representative of burst error channels. In the simulation, the fade margin for the 2-state channel model was 25 and the angle between the transmitter and the receiver was assumed to be 0°. Figures 8a and 8b show the results from 100,000 iterations and 50,000 iterations, respectively.

Finally, the performance of the whole system is shown in Figure 9 for the concatenated coding system with a BCH inner code and RS inner code in a Rician fading channel with the Doppler Effect. The inner decoder is the soft VA for BCH and the algebraic one for RS. Each result for the RS-VSD (K=5) case in Figure 9 was from 100,000 iterations. Each result for the other cases in Figure 9 was from 10,000 iterations. The K-factor is the ratio between the power in the direct path and the

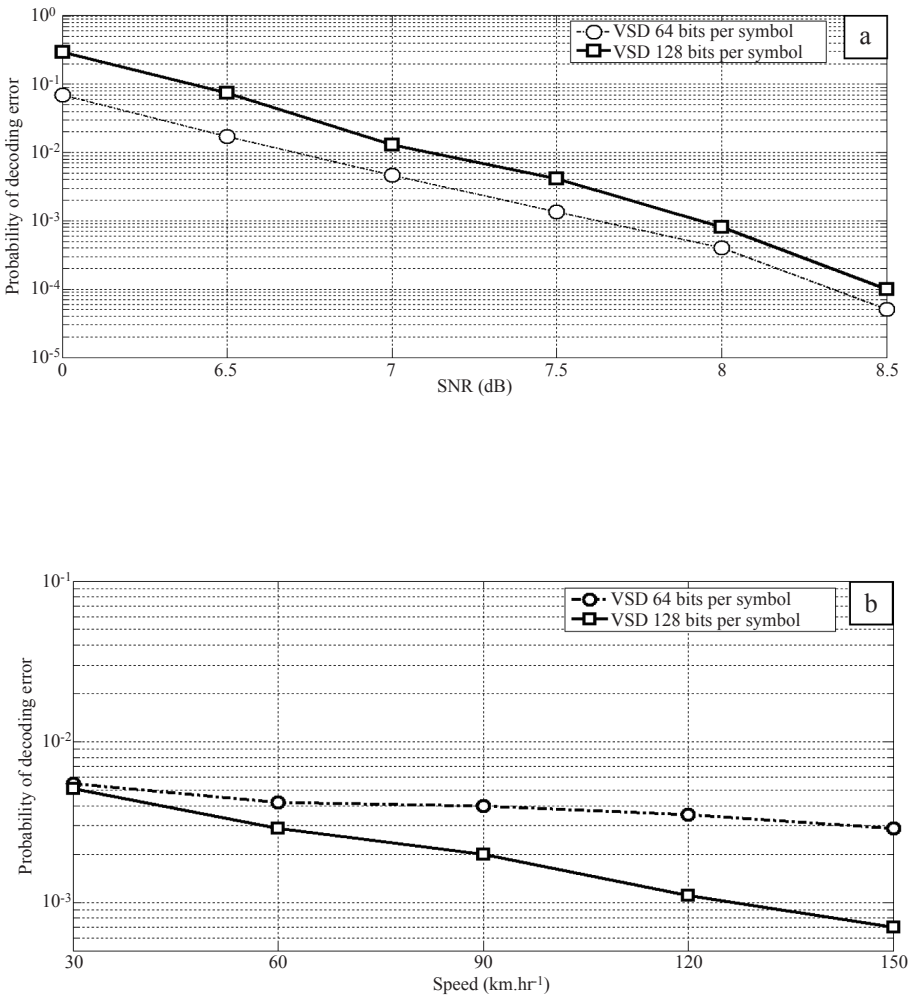

Figure 8 Decoding error probability of vector symbol decoding (VSD) only with no inner code with 64-bit and 128 bit symbols for: (a) AWGN channel; and (b) 2-State channel model. (SNR = Signal to noise ratio, AWGN = additive white Gaussian noise.)

other, scattered, paths. In the Rican channel with K = 3, 5 and f_d = 155.54 Hz, the RS system case provided much better performance than the BCH system case even when the RS decoder was a hard decision and the BCH decoder was a soft decision. For example, for an SNR of 11 dB and K = 5, P_e drops from 0.3 to 3×10^{-4} when the inner code was changed from the BCH to the RS code. In addition, the Rician example with K = 5 provides better performance than when K = 3 for all cases.

Hardware

Each hardware component was tested separately to confirm its functionality. The hardware results for the encoders and the List-of-2 soft VA were provided in Thonchai *et al.* (2013). The current study presents the result of VSD and the complete system with the RS inner code. Figures 10 and 11 show a test example. First, the connection was made between the Matlab program in the computer and the FPGA board via the Ethernet as shown in Figure 10a. Then the first two input data symbols to the (3,2,2) outer encoder were received. Each symbol was 102 bits represented as 13 bytes from "2" to "E" and "F" to "1B" in hexadecimal format. The outer encoder output consisted of 39 bytes (after "outer conv to rs" in Figure 10a). This output was sent to the RS encoder, which treated each group of 6 bits as an input symbol. Thus, there were 51 input symbols over GF(2^6). The output (after "Reed Solomon code" in Figure 10a) consisted of 63 symbols or 378 bits. Next, a 2-byte header "7E 7F" was added to the encoded symbols. Then, they were transmitted via the RS-232 port to the JZ863 transmitter module with frequency shift keying at 433 Mhz. The received data sequence is shown in Figure 10b. The RS inner decoder output is shown in Figure 11a and the VSD output is shown in Figure 11b.

The resource utilization on the Nanoboard 3000 model XC3S1400AN-4FGG676C (Table 1) was the same for the encoder and the decoder since they used the same design for the soft processor although the decoder was much more complicated than the encoder. Only 28% of the 4-input LUTs-logic, 36% of the I/O pin and 14% of the slice flip flops were used.

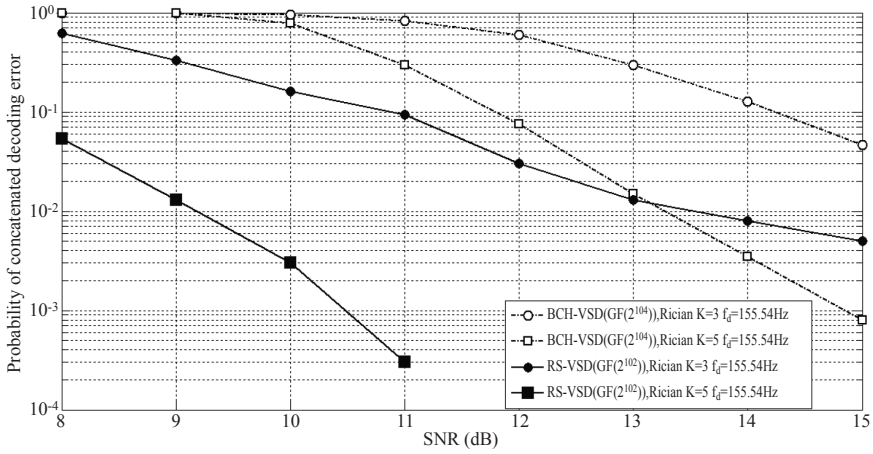

Figure 9 Performance comparison between Bose-Chaudhuri-Hocquenghem (BCH) and Reed-Solomon (RS) inner codes with vector symbol decoding (VSD) outer decoding in Rician fading channel. (GF = Galois field, SNR = Signal to noise ratio, f_d = Doppler spread, K = Rician K-factor, which is the ratio of signal power in the dominant component to the scattered power.)

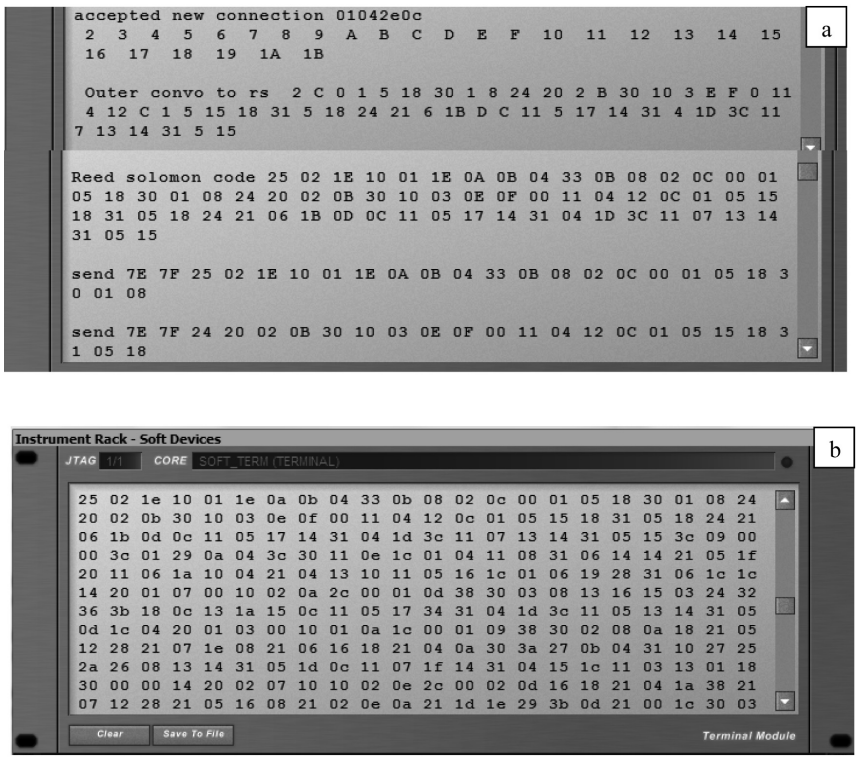

Figure 10 Soft terminal display for: (a) Encoders and (b) Received data.

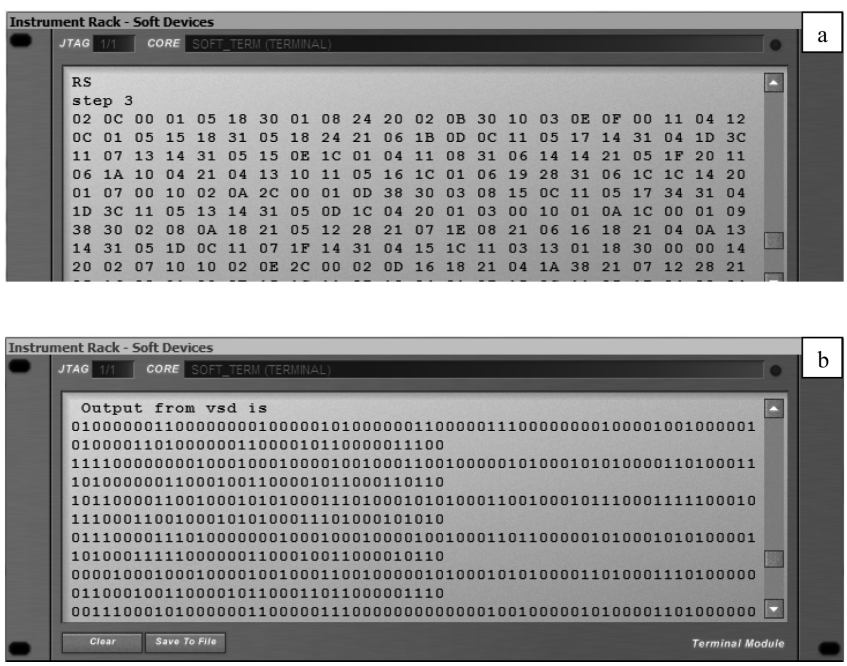

Figure 11 Soft terminal display for: (a) Reed-Solomon decoder output and (b) Vector symbol decoding output.

Table 1 Resource utilization with the same utilization for the encoder and the decoder.

Logic Utilization	Used	Total	% Usage
Number of slice flip flops	3,198	22,528	14%
Number of 4 input LUTs	6,509	22,528	28%
Logic distribution			
Number of occupied slices	4,194	11,264	37%
Total number of 4 input LUTs	6,853	22,528	30%
Number used as logic	6,253		
Number used as a route-thru	344		
Number used for Dual Port RAMs	256		
Number of bonded IOBs	183	502	36%
Number of BUFGMUXs	5	24	20%
Number of MULT18X18SiOs	2	32	6%
Number of RAM16BWes	18	32	56%

LUT = Look up table, RAM = Random access memory, IOB = Input / output bounds, BUFGMUX = Global clock MUX buffer with output state 0, MULT18X18SiO = 36-Bit output, 18×18-bit input dedicated signed multiplier, RAM16BWe = Byte-write enable support (Block RAM).

DISCUSSION

The results showed that the concatenated code with the inner RS code performed better than the one with the inner BCH code even if the first case used hard decision decoding, while the second case used soft decision VA. These results were for the mobile channel modeled with Rician fading and the Doppler Effect. The code rate for RS was 51/63 = 0.8095, while for BCH it was 26/31 = 0.8387. The outer symbol size for the RS case was 102 bits and for the BCH case was 104 bits. The code rate and the outer symbol size were selected to be close to each other although not the same in order to use the common BCH and RS codes.

At SNR = 11 and 15 dB in the Rician channel with K = 3 and the typical 3G carrier frequency of 2.1 GHz and 80 km.hr^{-1}, the concatenated code with the RS inner code was better than the BCH system by 88.59 and 89.25%, respectively. Similar results were also found for K = 5 cases because this RS code had a higher correction capability than the BCH code. For the inner decoding part only, the list soft VA for the selected BCH code was best in the AWGN channel. It was also better in the Rician than in the Rayleigh channels, both with and without the Doppler Effect. The performance was very similar for the different velocities (80 and 120 km.hr^{-1}) for both the Rician and Rayleigh channels. Hard decision was worse than all soft decision cases as expected. To improve the performance of the complete system further, list decoding may be used for both the BCH and RS inner codes. For the outer decoding part only, the larger sized symbols were preferred in a burst error channel and the smaller sized symbols in a random error channel.

As a result of using a soft core processor, the more complicated decoder and the simpler encoder used equal board resources due to the same design. It was much simpler to test new algorithms and systems using the soft processor than the design with the VHDL language. However, using VHDL will allow the hardware to operate faster than using a soft core processor with C language because VHDL is the IEEE standard hardware language that provides concurrent (or parallel) computing (IEEE, 2009), while C is a procedural language that runs each instruction sequentially (Vine, 2008).

CONCLUSION

A nonbinary concatenated code with an inner RS code and outer convolutional code was proposed. The outer code with a large symbol size became practical with the use of VSD. The inner RS code was selected to scale up the concatenated code to handle longer burst errors in high speed mobile communications. The complete system was implemented to show that all algorithms were practical in terms of complexity. The performance analysis shows that for a Rician fading channel with the Doppler Effect, the system with RS and hard decision was much better than the one with BCH and soft VA. In addition to the mobile channels, the power line channel also had problems with burst errors caused by the impulsive noise. Thus, VSD may also be applied to this channel. Future work should include using more practical and faster hardware, a performance comparison between the system with list decoding of BCH, RS and convolutional inner codes and the performance of VSD in an impulsive noise channel.

ACKNOWLEDGEMENTS

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