

# Half Flash 4-Bit (BCD) using New Current-Mode Algorithmic ADC

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## ABSTRACT

This paper presents a current-mode technique for the design of algorithmic ADC in half-flash 4-bit (BCD). This circuit can be converted to 4-bit output at each moment and multiple output bit numbers by serial connection. It uses attenuation current quantization level for quality improvement by using the active current mirror which is better than the cascade current mirror. The advantages and disadvantages of different current mirror structures for using in the ADC in half-flash (BCD) are discussed. Experimental results for using a 0.13  $\mu\text{m}$  CMOS process are reported, which is displayed capable to the slowest conversion time is less than 80 ns, 12.5 MHz, power consumption of 1 mw. input current of 0-100 $\mu\text{A}$  and 2.5V single supply. Its feasibility agrees with simulation results of PSPICE program. From simulation testing, the conversion rate is faster than other method.

**Key words:** Analog to digital Converter (ADC), active current mirror, current comparator, current injection, half flash (BCD)

## INTRODUCTION

The analog circuit designed technique was developed to work under current mode by using digital submicron CMOS technology (Vittoz,1985) to decrease voltage operation and to increase high speed by using CMOS ADCs, such as two-step flash (Carreira,1994), pipelined (Wu,1995) and algorithmic (David *et al.*,1990) under the high-speed requirement with high resolution and less energy consumed. All the three principles are brought to put under consideration in order to achieve the required characterization for ADC. High-speed analog to digital converter by flash and two-step flash is quite popular but cannot increase the number of bits at the output. The number of comparison bits has to be  $(2^N-1)$ , which are the output bits. So it needs the space

area and powers twice the number of output bits. For two-step flash, the speed conversion is low because of losing time of main circuit DAC implementation. In this paper, a high speed algorithmic ADC is proposed. The proposed ADC speed is higher than that reported by David *et al.* (1990) about four times because its conversion 4-bit per each moment with ten quantized level BCD and output is based on algorithmic ADC. When using current-mode techniques to represent the signal in analog-to-digital converter, voltage swing is reduced and operating speeds are higher. It is possible to use the injection current technique in the current mirror. A concept of half-flash 4-bit (BCD) using new current mode algorithmic ADC is shown in experimental results based on various approaches to investigate the advantages of the different performances.

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## THE CURRENT –MODE ADC

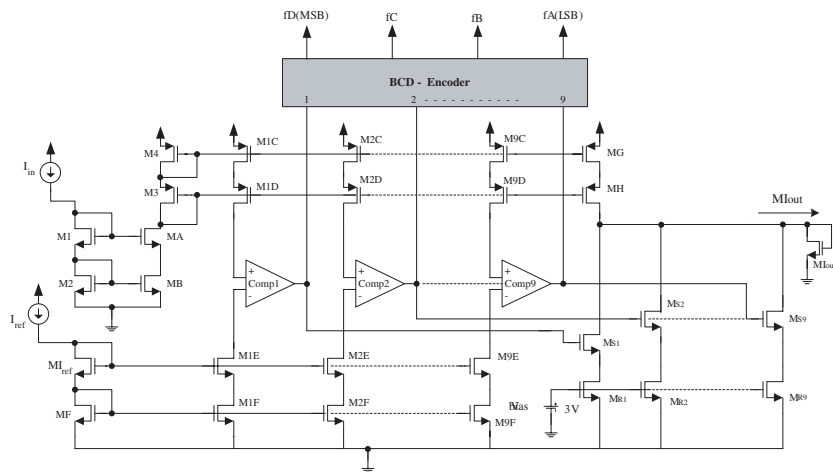
An algorithmic ADC (Nairn *et al.*,1990) for multiple bit output can be used by serial connection of each one-bit cell because a conversion time is created in association with desired multiple bit output if 4-bit ADC is used. In this paper, the circuit was designed to achieve 4-bit BCD output in each conversion time.

In Figure1, to solve the subtraction problem, the bit-cell (the input current  $I_{in}$  with the reference current  $I_{ref}$ ) in each of the current comparator (comp 1, comp 2,..., comp 9) respectively, the bit cell input voltage, even for extremely low currents, must be kept as high as possible while still maintain the highest possible

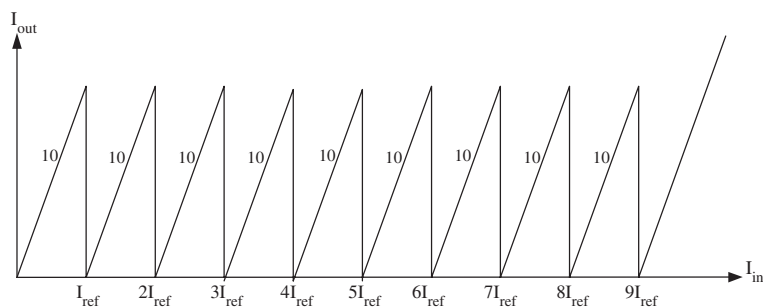
output resistance for each current mirror. Both objectives can be achieved by using cascaded current mirror that both M1E, M1F of comp 1, M2E, M2F of comp 2 to until M9E, M9F of comp 9 remain in saturation even when the analog output goes as low as  $2V_T$ , thereby ensuring that the output resistance of the reference mirror is high at all time. The disadvantages cascaded current mirrors significantly reduce the dynamic range and hence the resolution of the ADC, and errors due to the device finite output resistance are reduced by using the cascaded current mirrors.

Figure 3 is composed of

$\frac{I_{ref}}{10}, 2\left(\frac{I_{ref}}{10}\right), \dots, 9\left(\frac{I_{ref}}{10}\right)$  compared with the



**Figure 1** Schematic of half-flash 4-bit BCD using cascaded mirrors.

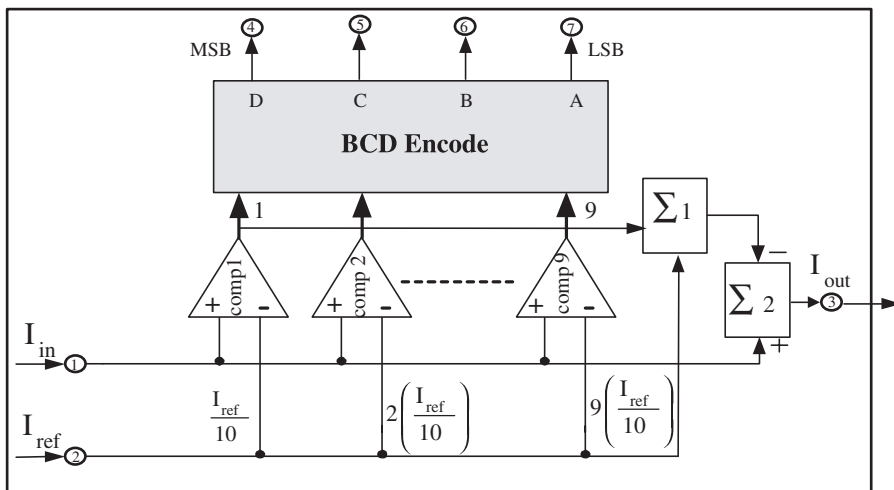


**Figure 2** Relation between  $I_{in}$  and  $I_{out}$ .

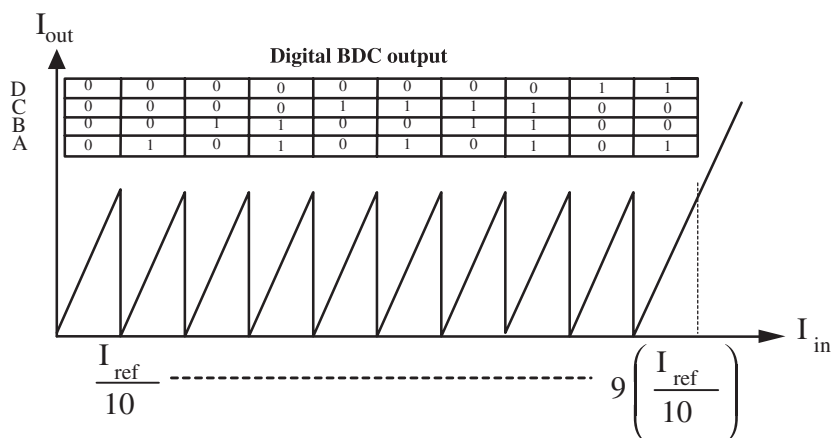
input current ( $I_{in}$ ). The BCD-encoder for encode the output comparator to BCD output at D, C, B, A output terminals, current summation circuit ( $\Sigma 1$ ), and current subtractor circuit ( $\Sigma 2$ ) operate as follows : the  $I_{in}$  is fed into circuit and compared the current with reference value of comparators comp1 to comp9. If  $I_{in}$  exceeds the reference current the output will be high. These outputs are encoded to binary code decimal by BCD-encoder and enable the summation of  $\Sigma 1$ . Therefore, the

output of  $\Sigma 1$  is zero if the comparators are zero. This output is fed to subtract with on  $\Sigma 2$  and will be in an output current ( $I_{out}$ ) or the analog signal.

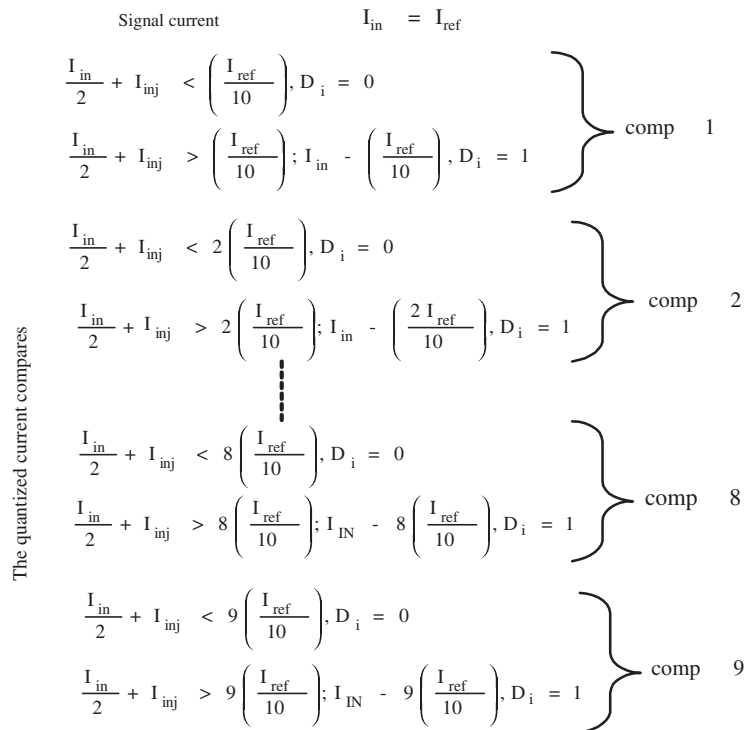
The current injection ( $I_{inj}$ ) technique (Fong *et al.*,1994, Tipsuvarnpron *et al.*,2005) in figure 6 can be used to speed up the current mirrors. The current injection reduces the input voltages swing and results in faster current mirror transient response in common with an attenuation of quantization current of ADC.



**Figure 3** Block diagram of new half-flash 4-bit BCD.



**Figure 4** Relation of new half-flash 4-bit BCD.



**Figure 5** The condition current compares of new half -flash BCD.

$$\begin{aligned} &\text{comp } 1; \left( \frac{I_{ref}}{10} \right); I_{ref} = 100 \mu A \\ &\left( \frac{100 \mu A}{10} \right) = 10 \mu A, \text{ assume } I_{inj 1 a} + I_{inj 1 b} \\ &I_{inj 1 a} = I_{inj 1 b} = 5 \text{ mA} \\ &\text{comp } 2; 2 \left( \frac{I_{ref}}{10} \right); I_{ref} = 100 \mu A \\ &2 \left( \frac{100 \mu A}{10} \right) = 20 \mu A, \text{ assume } I_{inj 2 a} + I_{inj 2 b} \\ &I_{inj 2 a} = I_{inj 2 b} = 10 \mu A \\ &\text{until to comp } 9 \text{ is} \\ &9 \left( \frac{100 \mu A}{10} \right) = 90 \mu A, \text{ assume } I_{inj 9 a} + I_{inj 9 b} + I_{inj 9 c} \\ &I_{inj 9 a} = I_{inj 9 b} = I_{inj 9 c} = 30 \mu A \end{aligned}$$

**Figure 6** The value of references current of new half -flash BCD.

## ACTIVE CURRENT MIRROR

The maximum multiple output bit of the purposed circuit is defined by error of current mirror (D.A.Freitas *et al.*,1983) which is usually no less than 1%. To correct that, the cascade current mirror can be used. But it reduces the input operation. Hence, the active current mirror has been used to improve for the output increment bit by non-reduced input operation range. For the active current mirror circuit in Figure 7, and its error shows in equation (1), where  $r_o$  is the output resistance of the previous stage and  $g_{m1}$  is the transconductance of transistor M1, (Usually,  $r_o \cong 5M\Omega$ ,  $g_{m1} \approx 20 \mu A/V$ ). When amplifier gain is to occur, the error of the active current mirror circuit is equal to 0.01 %.

$$I_{in} - I_{out} = \frac{1/Ag_{m1}}{r_o + 1/Ag_{m1}} \cong \frac{1}{Ag_{m1}r_o} \quad (1)$$

## CURRENT COMPARATOR CIRCUIT

The current comparator circuit is similar to current comparator circuit proposed in CADC (Nairn *et al.*,1990) which enables to control comparison in (Freitas *et al.*,1983) analyses the operation range and specified transistor

characteristic (Wang,1997). In operation, each comparator part will be separated. In Figure 8, the reference levels by bias voltage ( $V_{gs}$ ) of transistor Mnc1 to Mnc9 set threshold current equal  $I_{ref}$  to  $9I_{ref}$  respectively. The  $I_{in}$  on drain of transistor Mpc1 forces the drain current of Mpc1 to be equal to  $I_{in}$ . If this current exceeds the reference threshold current of  $I_{ref}$  the output of comp1 will be high ( $V_{dd}$ ), otherwise it will be low because the Mpc1 is active in linear region and active in saturation region. The relationship of output voltage can be written as follow:

$$V_{out} = \frac{1}{(g_{dpc1} + g_{dnc1})} (g_{mpc1} V_{gspc1} + g_{mnc1} V_{gsnc1}) \quad (2)$$

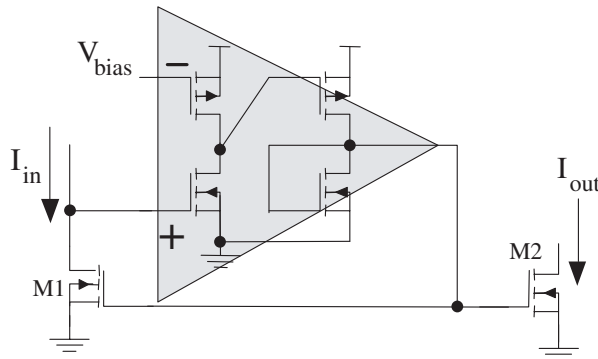
$g_{dpc1}$ ,  $g_{dnc1}$  is the gate drain voltage of pmos1 and nmos1.

$$\text{as } g_d = \lambda I_D ; g_m = \sqrt{2\mu C_{OX} \frac{W}{L} I_D}$$

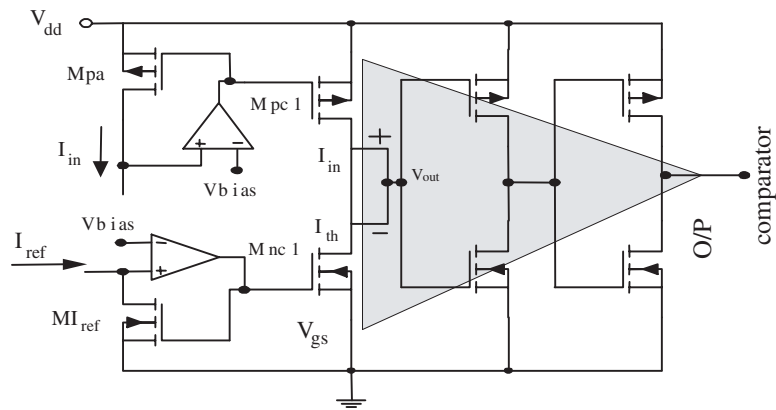
onto (3) than to get (4).

$$V_{out} \cong \frac{1}{(\lambda_p + \lambda_n)} \left( \frac{W_{pc1}}{L_{pc1}} - \frac{W_{nc1}}{L_{nc1}} \right) \quad (3)$$

We found that, in equation (3), the output can be set to high or low by controlling W/L ratio of  $M_p$  and  $M_n$  transistors on comparator circuit which comp 1, comp 2,..., comp 9 are set W/L to relate to  $I_{ref}$ ,  $2I_{ref}$ ,...  $9I_{ref}$ , respectively.



**Figure 7** Active current mirror.



**Figure 8** Current comparator circuit.

### BCD-ENCODER CIRCUIT

Principle of comparison as described in Table I can encode the comparator outputs to binary code decimal by reed-mulier minimization (Almaini in 1991). Therefore the D,C,B and A output can be written as equation (4),(5),(6) and (7) respectively.

$$D = \text{Comp } 8 \quad (4)$$

$$C = \text{Comp } 8 \oplus \text{Comp } 4 \quad (5)$$

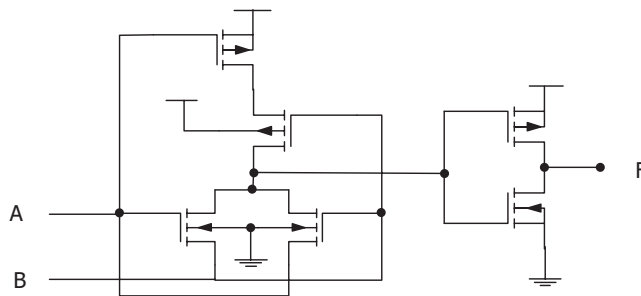
$$B = (\text{Comp } 2 \oplus \text{Comp } 4) + (\text{Comp } 6 \oplus \text{Comp } 8) \quad (6)$$

$$A = \text{Comp } 1 \oplus \text{Comp } 2 \oplus \dots \oplus \text{Comp } 9 \quad (7)$$

From equations (4) to (7) 48 MOS in passes transistor to BCD-encoder circuit is used. An exclusive-or gate in this equation with six MOS is illustrated in Figure 9.

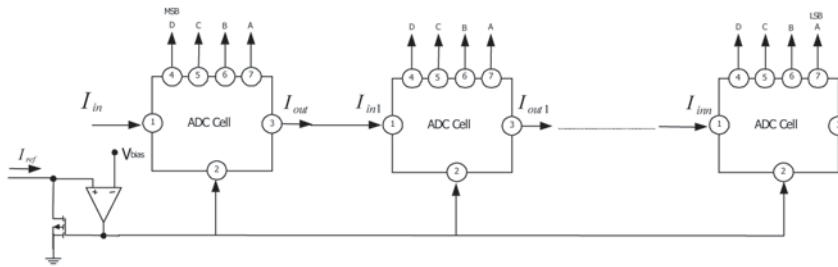
### A 4-BIT BCD HALF FLASH ADC

Figure 10 shows the integration of the proposed circuit. The input current is fed into drain of M1, which constructed in active current mirror forcing  $I_{D2}$  and  $I_D$  of Mpc1, Mpc2,..., Mpc9 to be equal  $I_{in}$ . This current is fed to input of comparators comp1, comp2,...,comp9 for comparing with references which are set to  $I_{ref}$ ,  $2I_{ref}$ ,...,  $9I_{ref}$  by W/L ratio of Mnc1, Mnc2,..., Mnc9 respectively. The output of comparators will be encoded by BCD- encoder and enable MOS switches (Ms1 to Ms9) for subtraction  $I_{in}$  which are stored as drain current of Mpc1 to Mpc9 with reference to each quantizing MOS (Mnc1 to Mnc9) which set values of  $I_{ref}$  to  $9I_{ref}$  respectively. The analog output current ( $I_{out}$ ) is residued from subtracted in the operation circuit.



**Figure 9** Exclusive-OR gate circuit.





**Figure 11** ADC connection of N-bit multiple circuit.

current mode algorithmic ADC operating from a 2.5 V has been designed and implemented. When the current-mode ADC presented above is compared to 2 techniques for designing ADCs. It is evident that the current-mode techniques offer half-flash 4-bit BCD favorable speed and low - power dissipation In particular the half-flash 4-bit BCD ADC using active current mirrors, current injection technique and new algorithmic current-mode ADC above can be operated half-flash 4-bit BCD by using cascaded mirrors. By optimizing the amplifier used in the active current mirrors and reducing the reference current, it is achieved with a power dissipation in the range.

## CONCLUSION

The method used with the current injection technique and attenuation quantized current in ADC yield advantages that speeding up transient response of the current mirrors and the other involves reducing power consumption. It reduces current mismatches due to the device. The finite output resistance is achieved not by increasing the output resistance itself but by reducing the mirror input resistance (advantage of the active current mirrors). The conversion accuracy depends on controllability of parameter that associates with W/L ratio in fabrication process. The conversion time is the function of mirror delay and switching speed of MOS transistor. Because the output is BCD; it is useful

to various digital electronic application designs and it can be seen that the current-mode ADC offers low power, and high conversion rates making it well suited for using in VLSI systems.

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