The Effect of Temperature on Threshold Voltage, The Low Field Mobilty and the Series Parasitic Resistance of PMOSFET

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ABSTRACT

This article describes the effect of temperature on the threshold voltage, low field mobility and S/D series parasitic resistance of PMOS over operating temperature range of 27 ^{0}C to 125 ^{0}C. The relation of I_{DS} and V_{GS} in a linear region was used with a different of channel length at a fixed value of channel width that effect of the channel width is excluded. The extraction procedure is based on the measurement of the transconductance characteristics of MOSFET in the linear region. The results show that, the temperature coefficient for threshold voltage is around 1.7mV/^{0}C approximately. The low field mobility degradation parameter is decreased by the factor of 0.68. The temperature coefficient of source-drain series resistance per unit channel width (R_{DSW}) is approximately 16.7 ohm-um/K. These data are necessary for the circuit designer to understanding well in the elevated operating temperatures.

Keywords: NMOS, PMOS, Threshold voltage

1. INTRODUCTION

The electrical characteristics of MOSFET normally are strong dependence on the operating temperature. One of the main parameter is the low field mobility that is decreased with temperature also the Φ_S and V_{FB} which are decreased with temperature. The threshold voltage (V_{TH}) is the first order important parameter that sensitive to the operating temperature. The threshold voltage is decreased as the temperature increase due to the Fermi-level and band gap energy shift. The threshold voltage depends linearly on the operating temperature for the long channel devices. The following temperature model of V_{TH} at zero substrate bias and current is used [1].

$$V_{TH}(T) = V_{TH}(T_{ref}, L, V_{DS}) + TCV \cdot \left(T - T_{ref}\right) \quad (1)$$

Where $V_{TH}(T_{ref},L,V_{DS})$ is a threshold voltage at specific L , V_{DS} measure at $T=T_{ref}$. The parameter TCV is the threshold voltage dependence with temperature with a unit of V/K.The temperature dependence on the mobility in BSIM3 is defined as

$$\mu(T) = \mu(T_{ref})\left(\frac{T}{T_{ref}}\right)^{UTE} \quad (2)$$

The drain current of MOSFET at a function of temperature is defined as

$$I_{DS}(T) = K(T)[((V'_{GS} - V_{TH}(T)) - 0.5V'_{DS}]V'_{DS} \quad (3)$$

$$K(T) = \frac{K_0(T)}{1 + \theta\ (V'_{GS} - V_{TH}(T))} \quad (4)$$

$$K_0(T) = K_0\left(T_{ref}\right)\left(\frac{T}{T_{ref}}\right)^{UTE} \quad (5)$$

$$K_0 = C_{ox}\frac{W_{eff}}{L_{eff}}U_o \quad (6)$$

$$V'_{GS} = V_{GS} - 0.5I_{DS}R_{DS} \quad (7)$$

$$V'_{GS} = V_{GS} - 0.5I_{DS}R_{DS} \quad (8)$$

$$\theta_m = \theta + K_0 R_{DS} \quad (9)$$

$$L_{eff} = L_{drawn} - 2dL \quad (10)$$

$$W_{eff} = W_{drawn} - 2dW \quad (11)$$

Where K_0 (A/V^2) is the maximum device transconductance parameter, T_{ref} is the nominal temperature or reference temperature at which parameters are extracted (27 ^{0}C), TCV is the threshold voltage temperature coefficient, Uo is the Low field mobility, θ is the mobility degradation

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factor, V_{TH} is the threshold voltage, UTE is temperature dependence on the low drain bias mobility, V_{TH} is the threshold voltage, W_{eff} is the effective channel width, L_{eff} is the effective channel length, dL is the channel length reduction on one side, dW is the channel width reduction on one side, C_{ox} is the gate oxide capacitance per unit area, R_S is a series parasitic resistance at the source end, R_D is a series parasitic resistance at the drain end, by assuming the R_D=R_S=R_{DS}/2. In BSIM3, the temperature dependence of the series S/D resistance is defined by

$$R_{DSW}(T) = R_{DSW}(T_{ref}) + PRT\left(\frac{T}{T_{ref}} - 1\right) \quad (12)$$

Where R_{DSW} is the parasitic series resistance per unit channel width exacted at T=T_{ref}, PRT is the temperature coefficient for R_{DSW}.

In this paper, we reported the effect of temperature on the basic electrical characteristics of PMOS devices in a supply voltage of 5.0 V. The temperature dependence of a device performance parameter such as the threshold voltage, the saturation drain current, low field mobility, mobility degradation and series parasitic resistance are determined. The buried channel PMOS devices is given that;

1) CMOS technology fabrication is the dominant technology in modern VLSI and PMOS device is part of the CMOS structure.

2) boron-ion implantation in the channel for VTA adjust is now commonly used in both NMOS and PMOS device in CMOS technology and this serves mainly to match on the threshold voltage of both devices. This channel doping process can be used to prevent the NMOS from exhibiting the punchthrough effect. However, it can cause the formation of the p-type buried channel in the enhancement mode PMOS device.

2. Experimental Procedure

A. *Devices Fabrication*

The PMOS test devices in this paper were fabricated by Twin-Well 0.8 CMOS technology (TMCN08) from Thai Micro Electronics Center (TMEC). They start with p-type substrate 25 Ω-cm of resistance. The N-well was form by phosphorus ion implantation with dose of 6×10^{12} cm^{-2} with a fixed energy of 140 keV for a conventional well that have a doping concentration of 3×10^{16} cm^{-3} with the junction depth was approximately 1.8μm . A self-aligned n+ poly silicon gate process 350 nm of thickness was used with gate oxide 15 nm of thickness. A BF_2^+ ion implantation with dose of 1×10^{12} cm^{-2} and 70 keV of energy for threshold voltage adjust process in a channel was implemented in order to match the threshold voltage of the NMOS and PMOS device as require in the modern CMOS technology process. As a result, a surface channel and a buried channel were formed in NMOS and PMOS respectively. There have no anti-punchthrough process for PMOS since the N-well concentration was high enough. Low energy implants are required to form shallow junctions self-aligned to the poly silicon gate. Phosphorus and BF_2 implants formed the lightly doped drain (LDD) of NMOS and PMOS devices. The BF_2^+ ion implantation with dose of 2×10^{13} cm^{-2} and a energy of 90 keV was used for the LDD implantation. The junction depth of LDD is around 0.2μm. An oxide spacer technology was used the LDD spacer.The spacer width is approximately 200 μm. The source and drain junction depth were approximately 0.3 μm with approximately 75 Ω/square of sheet resistance. The scalable device test structure have been design for different device geometries; Big dimension (W=20 μm, L= 20 μm) and short dimension (L= 0.6 μm, 0.7 μm 0.8 μm, 1.2 μm, 1.6 μm, 3.0 μm and 20 μm , W= 20 μm). The lateral diffusion is 0.06 μm/side and the channel width reduction is approximately 0.5 μm/side respectively. Fig. 1 shows the PMOS buried channel cross section from Sentaurus process simulation software.

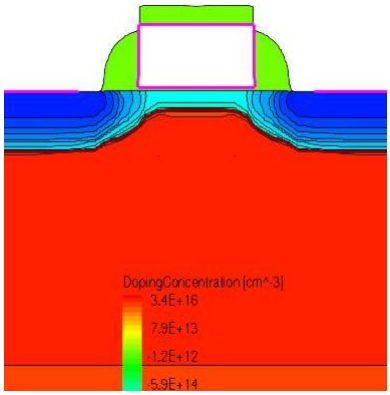


Figure 1. PMOS cross section from process simulation

In simulation, the n-well concentration is 3×10^{16} cm^{-3}, the channel concentration is approximately 3×10^{16} cm^{-3} with junction depth of 0.1μm. Figure 2 shows the scalable device of PMOS

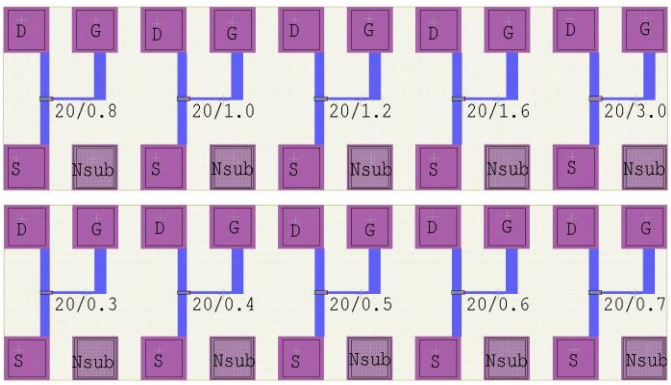


Figure 2. Illustration the PMOS device test structure

B. *Devices Measurement*

The threshold voltage measurements for testing device were performed by measuring a set of log I_{DS} versus V_{GS} by the linear extrapolation methodology. The most common threshold voltage measurement method is the linear extrapolation method using the maximum slope technique of I_{DS} and V_{GS} which the drain current is measured as a function of gate voltage at low drain voltage of typically 100 mV to ensure that the operation is in linear region. Hence, the I_{DS} versus V_{GS} is extrapolated at $I_{DS} = 0$ and the threshold voltage is determined from the extrapolated or intercepted gate voltage V_{GS} by V_{TH}= V_{GS}-0.5 V_{DS} as shown in Fig. 3.

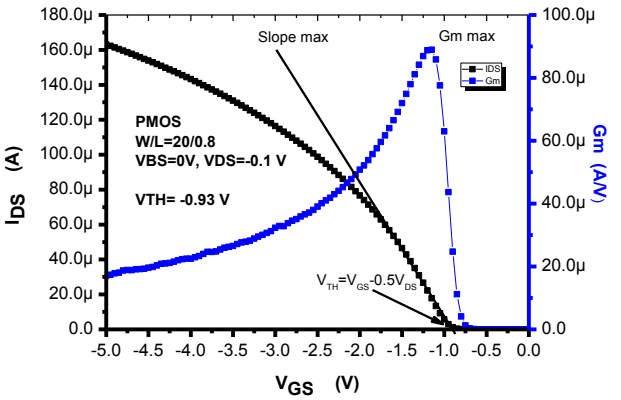


Figure 3. The threshold voltage measurement method of PMOS in linear region at temperature 27 °C

It is common to find the maximum slope on the I_{DS} versus V_{GS} by a maximum transcomductance, $Gm = \partial I_{DS}/\partial V_{GS}$. The intercept with the x-axis is taken as V_{TH}. In saturation region, the voltage is swept in order to find the maximum slope of the square root of the drain current as a function of the gate voltage [2].

$$\sqrt{I_{DS}}(T) = \sqrt{\mu(T)}\sqrt{\frac{1}{2}\frac{W_{eff}}{L_{eff}}C_{ox}}\left(V_{GS} - V_{TH}(T)\right) \qquad (13)$$

A linear extrapolation is performed around this operating point. The intercept with the x-axis is taken as V_{TH} as shown in Figure 4. The testing PMOS devices using a precision semiconductor parameter analyzer B-1500A with a thermal chuck in the range of 27 ^{0}C to 200 ^{0}C in manual operating.

Fig. 5 (a) shows log I_{DS} versus V_{GS} characteristics of PMOS and Fig. 5(b) shows I_{DS} versus V_{GS} characteristics of PMOS as the gate voltage V_{GS} was swept from 0 V to -5.0 V at zero substrate bias in the linear region (V_{DS}= -0.1V) in the range of 27 and 125 ^{0}C respectively. Fig. 6 shows the I_{DS} versus V_{DS} characteristics of PMOS as the drain voltage V_{DS} was swept from 0 V to -5.0 V at zero substrate and the gate voltage V_{GS} was swept from 0 V to -5.0 V (-1V/step) over the temperature in the range of 27 ^{0}C and 125 ^{0}C respectively.

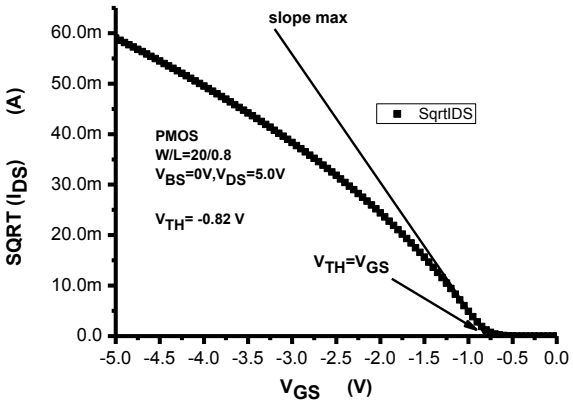
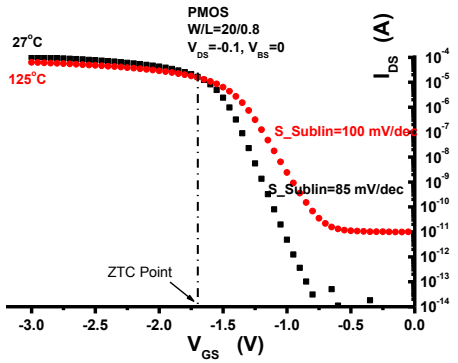
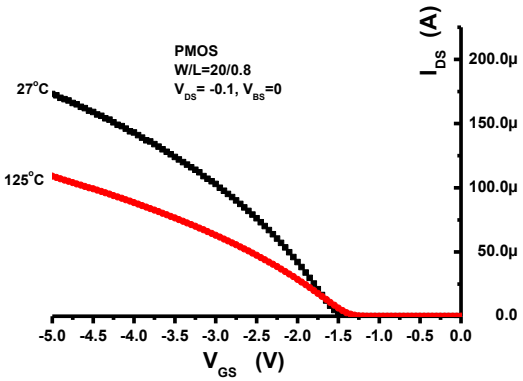


Figure 4. The threshold voltage measurement method of PMOS in saturation region at temperature 27 °C



(a)



(b)

Figure 5. (a) log I_{DS} versus V_{GS} and (b) I_{DS} versus V_{GS} of PMOS with temperature 27·C and 125·C respectively

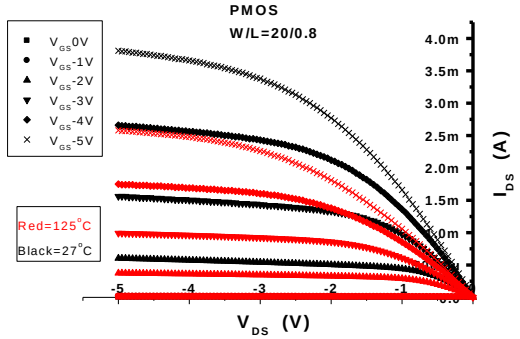


Figure 6. I_{DS} versus V_{DS} of PMOS with temperature 27 °C and 125 °C

C. Parameters Extraction

We can find the mobility degradation θ at the specific drawn channel length by plotting the relation between K_o and K of each specific channel length. the following equation was used for extraction.

$$\frac{K_0}{K} = 1 + \theta(V_{GS} - V_{TH}) \qquad (14)$$

Fig. 7 shows the extraction procedure of θ at 27 °C with drawn channel length of 20 µm

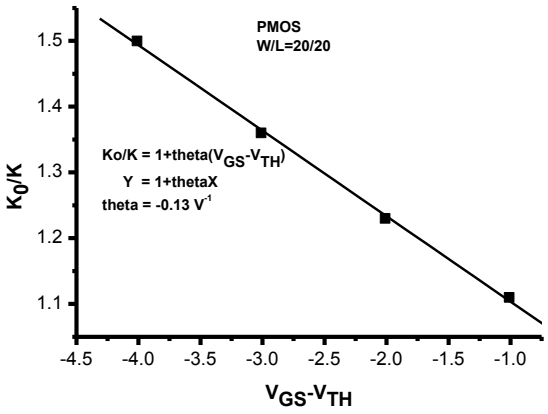


Figure 7. Extracted θ of PMOS with W=20 µm , L=20 µm at 27 °C

In Fig.7, the value of mobility degradation of a large PMOS is approximately -0.13 V^{-1}. As the channel length of testing devices are scaled down, the value of mobility degradation are increased as illustrated in TABLE I.

TABLE I. THETA OF PMOS AT VARIOUS TEMPERATURE AND W/L

W/L (um/um)	27^0C θ (V^{-1})	125^0C θ (V^{-1})
20/20	0.13	0.05
20/0.8	0.247	0.176
20/0.6	0.293	0.233

In TABLE I, we can find R_{DS} from the slope between θ & K_0 at a specific drawn channel length. In this graph, the y-intercept is a mobility degradation factor THETA (θ) and the slope is the series parasitic resistance as shown in Figure. 8.

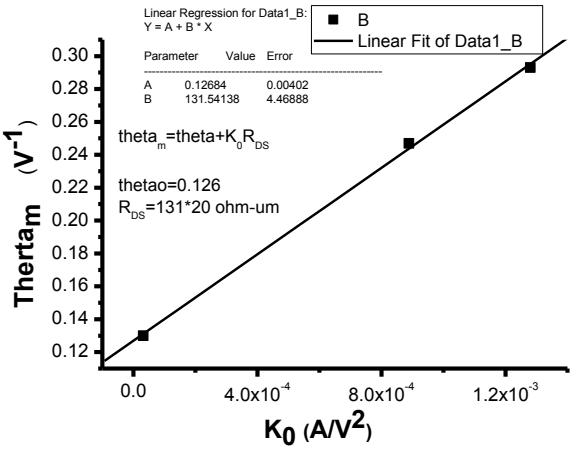


Figure 8. Extracted *THETA* versus K_0 of PMOS devices at 27 °C with drawn gate length of 20, 0.8 and 0.6 µm

3. RESULTS AND DISCUSSIONS

The mobility degradation factor *THETA* and R_{DS} at various temperatures as shown in Table II. In sub threshold region at given $V_{GS} \leq V_{TH}$, the drain current increased with operating temperature that caused by the junction current increased with the temperature and make the sub threshold current increased by the following relation; and also make the threshold voltage lowering with the operating temperature. In this region, the threshold voltage is a significant affected. The zero temperature coefficient point (ZTC) is a value -1.65 V of V_{GS} in linear region. The Subthreshold Swing in linear region (S_Subtlin) is around 85 mV/dec and 100 mV/dec at the temperature of 27 °C and 125 °C respectively. In saturation region, the The Subthreshold Swing in saturation region (S_Subsat) is around 88 mV/dec and 120 mV/dec at the temperature of 27°C and 125 °C respectively.

TABLE II THETA, K_o, U_0 AND R_{DS} OF PMOS AT VARIOUS TEMPERATURE AT W/L=20/20

Parameter	***27° C***	***125°C***	***unit***
Low Field mobility degradation (THETA, θ)	0.13	0.05	V^{-1}
Total Series Resistance (R_{DS})	2620	4260	Ω-um
Maximum Transconductance (K_0)	3.17×10^{-5}	1.0×10^{-5}	A/V^2
Low Field mobility (Uo)	138	94	cm^2/Vs

A small value of Subthreshold swing is desirable [10]. The drain leakage current at V_{GS}=0, V_{DS}=5.0V is approximately 2 decades increased. Above this point, the temperature effect on the mobility and series resistance is significant affected. Then, the drain current decreased as the operating temperature increased for all design drawn channel length. The effect of total parasitic series resistance makes the drain current is decreased as the operating temperature increased. This effect caused by the degradation of carrier mobility and the positive dependent of drain/source resistance on the temperature. The saturation drain current is decreased as the temperature increases by the factor of 0.68.The drain saturation current model over the operating temperature of a testing device can be defined as

$$I_{DS}(T) = I_{DS}(Tref)\left[1 + TCI_{DS}(T - T_{ref})\right] \quad (15)$$

TCI_{DS} is a coefficient of drain saturation current over the operating temperatures that have a value of -0.33 %/K. Fig.5 shows the threshold voltage versus mask channel length width an operating temperature as a parameter. It can be seen that, the threshold voltage decrease rapidly for the mask channel length lower than 0.8 μm for all operating temperature.
The coefficient of threshold voltage over the operating temperature is 1.7mV/K. The threshold voltage model over the operating temperature of a testing device can be defined by

$$V_{TH}(T) = V_{TH}(T_{ref}, L, V_{DS.0.1}) + 1.7\times10^{-3}(T - T_{ref}) \quad (16)$$

The process tranconductance or the low field mobility is decreased as the temperature increases by the factor of 0.68. The model over the operating temperature can be extracted by the relation

$$\ln K(T) = \ln K(T_{ref}) + UTE[\ln(T) - \ln(T_{ref})] \quad (17)$$

The parameter UTE is extracted from the slope. The low field mobility model of long channel can be defined as

$$U_0(T) = 138\left(\frac{T}{T_{ref}}\right)^{-1.35} \quad (18)$$

Similarly, the process transconductance can be defines by

$$K(T) = 3.17\times10^{-5}\left(\frac{T}{T_{ref}}\right)^{-1.35} \quad (19)$$

The drain source series parasitic resistance per unit channel width (R_{DSW}) are extracted by I_{DS} versus V_{GS} of PMOS at various drawn channel length [7] at the temperature of 27 and 125 °C and also can be defined as

$$R_{DSW}(T) = 2620 + 5\times10^{3}\left(\frac{T}{T_{ref}} - 1\right) \quad (20)$$

4. CONCLUSION

The experimental results of the characterization of PMOS at elevated temperature fabricated in 0.8 μm CMOS process are presented. We note that an increase in temperature results in decrease of the threshold that caused by the increase of conduction current of MOSFET devices. On the other hand, the threshold slope is decreased with the temperature that caused by the increase of conduction current. The coefficient of threshold with temperature is in the range of 1.7 mV/K and 2.0mV/K in linear and saturation region respectively. The low field mobility decreases as the temperature increases by the factor of 0.68. The coefficient of drain saturation current over the operating temperatures have a value of -0.33 %/K. The mobility degradation parameter is drop linearly in rate of 8.2×10^{-4} V^{-1}/K. On the other hand, the series parasitic resistance per unit width is increased linearly by16.7 Ω.μm/K. These data are necessary for the circuit designer and process development to understanding well in the elevated operating temperatures. The new process and design for improvement will be discussed later on.

APPENDIX A

The drain equation excluded drain source series parasitic resistance is defined by

$$I_{DS} = K(V_{GS}^{/} - V_{TH})V_{DS}^{/} - 0.5V_{DS}^{/})V_{DS}^{/} \quad (A.1)$$

$$I_{DS} = K(V_{GS}^{/} - V_{TH})V_{DS}^{/} - 0.5V_{DS}^{/2}) \quad (A.2)$$

Where

$$V_{GS}^{/} = V_{GS} - I_{DS}R_S \quad (A.3)$$

$$V_{DS}^{/} = V_{DS} - I_{DS}R_{DS} \quad (A.4)$$

If $R_S = R_D = \frac{R_{DS}}{2}$

Then

$$V_{GS}^{/} = V_{GS} - 0.5I_{DS}R_{DS} \quad (A.5)$$

In linear region, the drain equation can be expressed by

$$I_{DS} = K(V_{GS}^{/} - V_{TH})V_{DS}^{/} \quad (A.6)$$

The equivalent circuits of MOS as show in figure A1

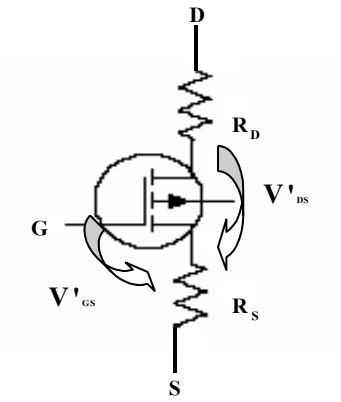


Figure A1. The equivalent circuit of MOS

The equation that combines drain source parasitic resistance is expressed as

$$I_{DS} = K\left[(V_{GS} - 0.5I_{DS}R_{DS}) - V_{TH}\right](V_{DS} - I_{DS}V_{DS}) \quad (A.7)$$

$$I_{DS} = K\left[(V_{GS} - V_{TH} - 0.5I_{DS}R_{DS})\right](V_{DS} - I_{DS}V_{DS}) \quad (A.8)$$

In strong inversion, $(V_{GS} - V_{TH}) \gg 0.5I_{DS}R_{DS}$

The final equation that combines drain source parasitic resistance can be expressed as

$$I_{DS} = K(V_{GS} - V_{TH})(V_{DS} - I_{DS}R_{DS}) \quad (A.9)$$

The next parameter is included in the model is mobility degradation.

$$K = \frac{K_0}{1 + \theta(V_{GS} - V_{TH})} \quad (A.10)$$

Where K_0 (A/V^2) is the maximum device transconductance parameter, θ is the mobility degradation parameter.The equation included the mobility degradation and series parasitic resistance can be expressed by the following

$$I_{DS} = K(V_{GS} - V_{TH})(V_{DS} - I_{DS}R_{DS}) \quad (A.11)$$

$$I_{DS} = KV_{DS}(V_{GS} - V_{TH}) - KI_{DS}R_{DS}(V_{GS} - V_{TH}) \quad (A.12)$$

$$I_{DS} + KI_{DS}R_{DS}(V_{GS} - V_{TH}) = KV_{DS}(V_{GS} - V_{TH}) \quad (A.13)$$

$$I_{DS}[1 + KR_{DS}(V_{GS} - V_{TH})] = KV_{DS}(V_{GS} - V_{TH}) \quad (A.14)$$

$$I_{DS} = \frac{KV_{DS}(V_{GS} - V_{TH})}{[1 + KR_{DS}(V_{GS} - V_{TH})]} \quad (A.15)$$

$$I_{DS} = \frac{\frac{KoV_{DS}(V_{GS} - V_{TH})}{1 + \theta(V_{GS} - V_{TH})}}{[1 + \frac{Ko}{1 + \theta(V_{GS} - V_{TH})}R_{DS}(V_{GS} - V_{TH})]} \quad (A.16)$$

$$I_{DS} = \frac{\frac{KoV_{DS}(V_{GS} - V_{TH})}{1 + \theta(V_{GS} - V_{TH})}}{\frac{[1 + \theta(V_{GS} - V_{TH}) + KoR_{DS}(V_{GS} - V_{TH})]}{1 + \theta(V_{GS} - V_{TH})}} \quad (A.17)$$

$$I_{DS} = \left[\frac{KoV_{DS}(V_{GS} - V_{TH})}{1 + [\theta(V_{GS} - V_{TH}) + KoR_{DS}(V_{GS} - V_{TH})]}\right] \quad (A.18)$$

$$I_{DS} = \left[\frac{KoV_{DS}(V_{GS} - V_{TH})}{1 + [(\theta + KoR_{DS})(V_{GS} - V_{TH})]}\right] \quad (A.19)$$

Let's assume that $\theta_m = \theta + KoR_{DS}$ the equation combined the SD series parasitic and mobility degradation can be defined as

$$I_{DS} = \left[\frac{K_o V_{DS} (V_{GS} - V_{TH})}{1 + [\theta_m (V_{GS} - V_{TH})]} \right] \quad \text{(A.20)}$$

We can find the mobility degradation θ and SD series parasitic resistance by the following procedure [4]. Where K_o is the slope max of I_{DS}& V_{GS}, K is the slope of I_{DS}& V_{GS} at a specific V_{GS}. We can find θ at the specific drawn channel length by plotting the relation between K_o and K. Use (A10a), we can find R_{DS} from the slope between θ_m & K_0 of each specific device that varying the channel length. And the y-intercept of θ_m & K_0 is a mobility degradation factor THETA (θ) of MOSFET. As you seen that the longer channel length value the lower mobility degradation value.

Appendix B

The series parasitic resistance at Drain side can be expressed as

$$R_D = R_{\square} \frac{L_D}{W_D} + R_{Cont} \quad \text{(B.1)}$$

Similarly, the series parasitic resistance at Source side can be expressed as

$$R_S = R_{\square} \frac{L_S}{W_S} + R_{Cont} \quad \text{(B.2)}$$

Where L_D is the length of Drain region, W_D is the width of Drain region, L_S is the length of Source region, W_S is the width of Source region, $R_{\square}$ is the sheet resistance of Drain/Source region and R_{Cont} is the contact resistance. The above parameters are illustrated in Figure A2.

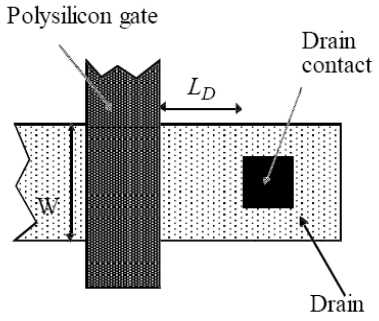


Figure A2. Layout design of MOS

The total series parasitic resistance included at Drain side and Source side is simplified as

$$R_{DS} = R_D + R_S$$
$$R_{DS} = R_{\square} \left(\frac{L_D}{W_D} + \frac{L_S}{W_S} \right) + 2R_{Cont} \quad \text{(B.3)}$$

In layout design, $W_D = W_S$, $L_D = L_S$
Then the total series parasitic resistance of both sides is expressed as

$$R_{DS} = R_{\square} \left(\frac{2L_D}{W_D} \right) + 2R_{Cont} \quad \text{(B.4)}$$

If we have multiple contacts in Drain and Source side, then the contact resistance at one side is defined as

$$R_{Cont} = \frac{R_{Cont}}{n} \quad \text{(B.5)}$$

Where n is the total number of contacts.

Acknowledgment

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