Current Applied Science and Technology Vol. 22 No. 3 (May-June 2022)

Research article

Gamma-radiation Induced Degradation of the Electrical Characteristics of NMOSFETs

Anucha Ruangphait[1], Amonrat Kerdpradist[2], Rangson Muanghlua[2]* and Yothin Wongprasert[2]

[1]Thai Micro Electronics Center, National Science and Technology Development Agency, Pathumthani, Thailand
[2]Department of Electronics Engineering, Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok, Thailand

Received: 1 February 2021, Revised: 7 July 2021, Accepted: 1 September 2021

DOI: 10.55003/cast.2022.03.22.004

Keywords

NMOSFETs;
threshold voltage;
gamma radiation;
device parameters

Abstract

In this paper, we present the gamma-radiation induced degradation of the electrical characteristics of N-channel Metal Oxide Semiconductor Field Effect Transistors (NMOSFETs). The exposure was done with a ^{60}Co gamma-ray source over the total dose range of 1 kGy to 10 kGy, with a dose rate of 3.9 kGyhr. The effects of irradiation induced degradation on device parameters such as threshold voltage, low field mobility, device transconductance (G_m), saturation drain current, off state leakage current and subthreshold swing were investigated. The threshold voltage was determined using the linear extrapolation method. The device dimensions with Wide/Long channel that excluded the Narrow Channel Effect (NCE) and the Short Channel Effect (SCE) were measured. The results showed that the threshold voltage, device transconductance and low field mobility decreased but the saturation drain current, off state leakage current and subthreshold swing increased as the gamma irradiation increased. Finally, the macro parameter models were investigated and discussed.

1. Introduction

Gamma radiation (γ-rays) is a type of high-energy electromagnetic wave arising from the radioactive decay of atomic nuclei. Gamma radiation or gamma ray (symbol γ) is a penetrating form of electromagnetic radiation. It consists in very short wavelength electromagnetic waves and so imparts very high photon energy. The physical properties of gamma radiation are short electromagnetic wavelengths in the range of 10^{-14} m → 10^{-10} m [1]. The radiation causes degradations in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) performance

*Corresponding author: Tel.: (+66) 9825949000
E-mail: rangson.mu@kmitl.ac.th

[2-4]. These degradations include an increase in leakage current, bulk resistivity, space charge concentration, and charge trapping. In Metal Oxide Semiconductor (MOS) structure, the ionization damage also creates trapped charges at the Si/SiO_2 interface. This trapping results in an increase of the oxide positive trapped charge with degradation of the SiO_2 dielectric layer. The most important parameter of NMOSFETs that are affected by the gamma radiation is the threshold voltage. The threshold voltage V_{TH} and can be represented as follows [5].

$$V_{TH} = \Psi_{MS} + 2\Phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \tag{1}$$

Where Ψ_{MS} is the metal semiconductor work function difference, Φ_F is the Fermi level, Q_B is the depletion charge by inversion per unit area, Q_{ox} is the effective total charge in the SiO_2, and C_{ox} is the capacitance per unit area of the SiO_2. The irradiation has no effect on Ψ_{MS}, Φ_F and Q_B. The relation between Q_{ox} and the threshold voltage is given by:

$$\Delta V_{TH} = -\frac{\Delta Q_{ox}}{C_{ox}} \tag{2}$$

The current of NMOSFETs can be defined by:

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} \left[\left((V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right) \right] \tag{3}$$

In the linear region: V_{DS} is small (V_{DS}=50 mV), and the drain current can be defined as:

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} V_{DS} (V_{GS} - V_{TH}) \tag{4}$$

Where μ_{eff} is the effective channel mobility, W is the channel width, L is the channel length, V_{DS} is the drain-source bias voltage. The subthreshold current between the drain and source occurs in NMOSFETs when the V_{GS} is below V_{TH} and can be modeled as [2]:

$$I_{sub} = I_o \exp\left(\frac{V_{GS} - V_{TH}}{m(v_T)} \right) \left(1 - \exp\left(\frac{-V_{DS}}{v_T} \right) \right) \tag{5}$$

The off state leakage current (I_{off}) is defined by the subthreshold current at 0 V of V_{GS} and 5 V of V_{DS}. Thus, the term $\left(1 - \exp(-V_{DS} / v_T\right)$ can be neglected. Then the off state leakage current can be described as follows:

$$I_{off} = I_o \exp\left(\frac{-V_{TH}}{m(v_T)} \right) \tag{6}$$

$$I_o = \mu_{eff} C_{ox} \frac{W}{L} (v_T)^2 \exp(1.8) \tag{7}$$

Where v_T is the thermal voltage given by kT/q, γ is the body effect coefficient, V_{DS} is the drain-source bias voltage, η is the DIBL coefficient, and m is the subthreshold swing coefficient. The

subthreshold swing (S) is the inverse slope of $\log_{10}(I_{DS})$ - V_{GS} curve. The subthreshold swing (S) is defined by [2]:

$$S = \left(\frac{d \log_{10}(I_{DS})}{d(V_{GS})} \right)^{-1} = \log(10) \frac{mkT}{q} = 2.3 \frac{mkT}{q} \tag{8}$$

$$m = 1 + \frac{C_D}{C_{ox}} + \frac{C_{IT}}{C_{ox}} \tag{9}$$

$$S = 2.3 \left(1 + \frac{C_D}{C_{ox}} + \frac{C_{IT}}{C_{ox}} \right) \frac{kT}{q} \tag{10}$$

$$N_{IT} = \frac{C_{IT}}{q} \tag{11}$$

Where C_D is the capacitance of the depletion region, C_{IT} is the interface state capacitance, k is the Boltzmann constant, N_{IT} is interface trap density given in a unit of cm^{-2}/eV, and q is the charge of the electron. A low subthreshold swing is desirable. The subthreshold slope indicates how effectively the MOSFET device can be turned off (decrease rate of I_{off}) when V_{GS} is decreased below V_{TH}.

The purpose of this paper is to investigate the degradation of the electrical properties of the NMOSFETs such as threshold voltage, on state current, off state current, and also the subthreshold swing. In addition, the effective total charge in the SiO_2 (Q_{ox}) and the interface trap density (N_{IT}) can also be determined from the threshold voltage shift and the subthreshold swing shift in the future.

2. Materials and Methods

The devices were designed and fabricated at Thai Micro Electronics Center (TMEC) in 0.8 µm Complementary Metal Oxide Semiconductor (CMOS) technology fabrication [6], starting with p-type substrate of 25 Ω-cm. A self-aligned n+ polysilicon gate process was used, and the Short Channel Effect (SCE) and the Narrow Channel Effect (NCE) were excluded. The dimension W/L=20µm /20µm was used and measured. The process parameters are listed in Table 1.

Table 1. Device parameters

Parameters	Value	Unit
P-Substrate Sheet Resistance	2000	Ω/Sq
N+ Active Sheet Resistance	50	Ω/Sq
N+ Active Junction Depth	0.4	µm
P+ Active Sheet Resistance	90	Ω/Sq
P+ Active Junction Depth	0.4	µm
N+ Poly Gate Sheet Resistance	30	Ω/Sq
N+ Poly Gate Sheet Thickness	3500	Å
Gate Oxide Thickness	15	Å

The layout design of NMOSFET using the Tanner Tool software is shown in Figure 1. The testing systems included a precision semiconductor parameter analyzer B-1500A, and a semi-automatic probe station cascade ALESSI REL6100 model. The I_{DS}-V_{GS} and G_m-V_{GS} of Wide channel width per Long channel length W/L=20µm /20µm for the threshold voltage extraction is shown in Figure 2. The log (I_{DS})-V_{GS} of NMOSFETs for V_{GS} varying from -0.2 V to 1.2 V for subthreshold swing (S) extraction is shown in Figure 3. The I_{DS}-V_{DS} of Wide/Long channel NMOSFET pre and after irradiation is illustrated in Figure 4. The I_{on}/I_{off} versus irradiation dose for NMOSFETs with the dimension W/L=20 µm/20µm is shown in Figure 5.

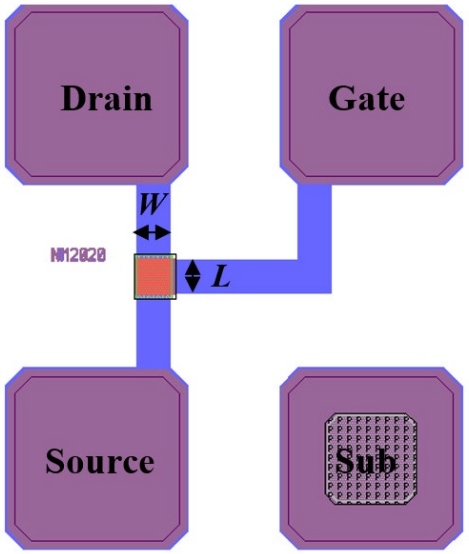

Figure 1. Design Lay out of Wide/Long channel NMOSFETs

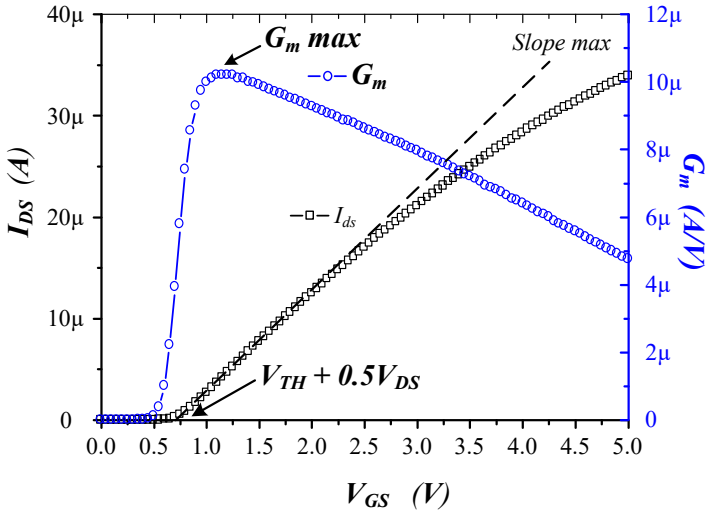

Figure 2. I_{DS}-V_{GS} and G_m-V_{GS} of Wide/Long channel NMOSFETs for V_{TH} extraction

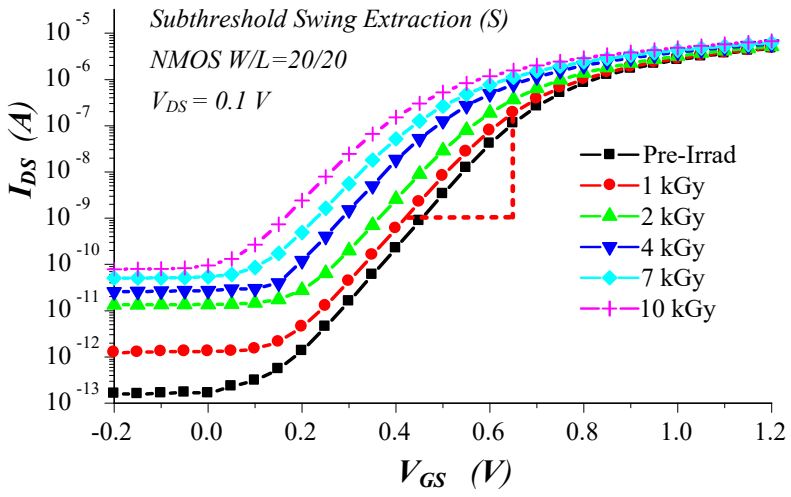

Figure 3. Log (I_{DS})-V_{GS} of Wide/Long channel NMOSFETs for subthreshold swing extration

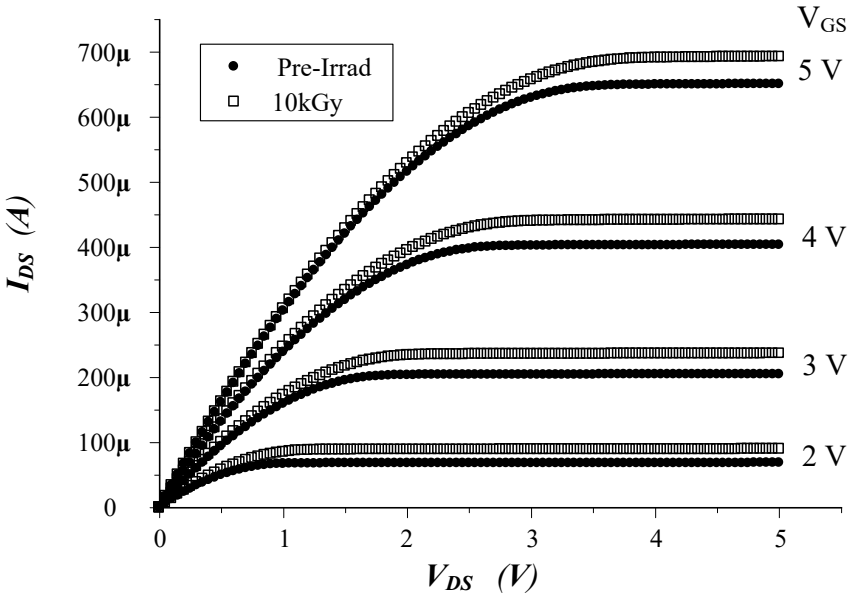

Figure 4. I_{DS}-V_{DS} of Wide/Long channel NMOSFETs pre-irradiation (black circle symbol) and after

irradiation 10 kGy (square symbol)

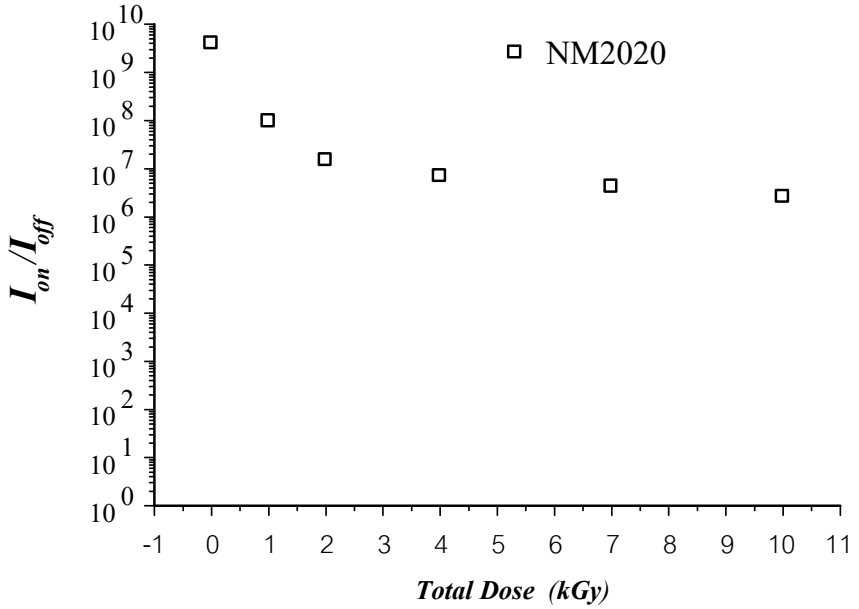

Figure 5. I_{on}/I_{off} pre and after irradiation of Wide/Long channel NMOSFETs

3. Results and Discussion

As can be seen in Figure 2, the results showed that the V_{TH} of pre-irradiated NMOSFETs was 0.69 V. After irradiation at the total doses of 1 kGy, 2 kGy, 4 kGy, 7 kGy and 10 kGy, the V_{TH} values were 0.67 V, 0.62 V, 0.55 V, 0.51 V and 0.45 V, respectively. Then, the threshold voltage shift was about -0.24 V or -24.0 mV/kGy at the total dose level of 10 kGy, mainly due to the increase of positive oxide trapped charge. The maximum transconductance (G_m) of pre-irradiated NMOSFETs was 10.21×10^{-6} A/V and the calculated low field mobility (μ) was approximately 468 $cm^2/V{\cdot}s$. The calculated G_m had a value of 9.64×10^{-6} A/V at the total dose level of 10 kGy. Similarly, the low field mobility (μ)decreased to 447 $cm^2/V{\cdot}s$ at the total dose level of 10 kGy.

In Figure 3, the subthreshold swing (S) was estimated from a linear regression logarithm of drain current (I_{DS}) in the interval level between 10^{-7} A and 10^{-9} A. The subthreshold swing (S) of pre-irradiated NMOSFETs was 95 mV/dec. The subthreshold swing (S) was found to increase to 98 mV/dec, 100 mV/dec, 102 mV/dec, 104 mV/dec and 107 mV/dec at the total doses of 1 kGy, 2 kGy, 4 kGy, 7 kGy and 10 kGy, respectively. The irradiation induced the interface trapped charge or the interface state capacitance (C_{IT}), causing the subthreshold swing (S) increase. The saturation drain current (I_{DS} at $V_{DS} = V_{GS} = 5$ V) of the Wide/Long channel was found to have increased from 650×10^{-6} A to 692×10^{-6} A at total dose of 10 kGy or it had increased by around 7% at the highest dose level of 10 kGy. The off state leakage current (I_{DS} at $V_{DS} = 5$ V, $V_{GS} = 0$ V) was found to have increased from the order level of 10^{-12} A to the order level of 10^{-10} A at irradiation of 10 kGy. The I_{on}/I_{off} ratio changed rapidly from 0 kGy to 2 kGy and I_{on}/I_{off} ratio changed slowly from 2 kGy to 10 kGy.

4. Conclusions

In this paper, the gamma-radiation induced degradation of the electrical characteristics of NMOSFETs was presented. The Wide/Long channel NMOSFETs were fabricated and measured. The threshold voltage was extracted from the linear extrapolation method. The irradiation exposure was done by a ^{60}Co gamma-ray source in the total dose range of 1 to 10 kGy at a dose rate of 3.9 kGy/hr. The results show that the threshold voltage (V_{TH}), the device transconductance (G_m) and the low field mobility (μ) decreased. However, the off state leakage current (I_{off}) parameter, the saturation drain current (I_{on}) and the subthreshold swing (S) increased. The above parameters made the saturation drain current of the tested NMOSFETs increased by approximately 7%. The off state leakage current increased by approximately 2 orders at the total irradiation value of 10 kGy. The degradation of the gamma irradiation NMOSFETs was mainly caused by the oxide trapped charge and the interface trapped charge, and this was mainly indicated by the investigation of threshold voltage shift and subthreshold swing.

5. Acknowledgements

The authors would like to thank the staff members of Thai Microelectronics Center (TMEC) for device fabrication. The Thailand Institute of Nuclear Technology approved access to irradiation facilities and the technicians provided technical assistance.

References

[1] World Health Organization, 2020. *Ionizing Radiation Dose and Source.* [online] Available at: https://www.who.int/ionizing_radiation/about/what_is_ir/en/index2.html.

[2] Roy, K., Mukhopadhyay, S. and Mahmood-Meimad, H., 2003. Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits. *Proceedings of the IEEE*, 91(2), 305-327.

[3] Barnes, C.E., Fleetwood, D.M., Shaw, D.C. and Winokur, P.S., 1992. Post irradiation effects (PIE) in integrated circuits. *IEEE Transactions on Nuclear Science*, 39(3), 328-341.

[4] Messenger, G.C. and Ash, M.S., 1986. *The Effect of Radiation on Electronic Systems*. New York: Van Nostrand Reinhold Inc.

[5] Gray, P.R. and Meyer, R.G., 1993. *Analysis and Design of Analog Integrated Circuits*. New York: John Wiley & Sons.

[6] Ruangphanit, A. and Muanghlua, R., 2012. The effects of temperature and device dimension of MOSFETs on the DC characteristics of CMOS inverter. *Proceedings of the 9th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology,* Phetchaburi, Thailand, May 16-18, 2012, pp. 341-345.