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Research article

PMMA/High-*k* Self-assembled TiO_2 /PMMA Multi-layer Gate Dielectric for P3HT Organic Field Effect Transistors

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Abstract

Keywords

organics field-effect transistors;

dielectric constant;

TiO_2;

PMMA;

P3HT

In this work, a multi-layer structure of poly(methyl methacrylate)/ titanium dioxide/poly(methyl methacrylate) (PMMA/TiO_2 /PMMA; PTP) was proposed as a top-gate insulator for P3HT-based organic field-effect transistors (OFETs). Adding a TiO_2 interlayer as a high dielectric constant (high-*k*) material into PMMA film enables the modification of the dielectric constant of the multi-layers PTP film. The content of TiO_2 in the PTP film, which can be varied by changing the number of soaking cycles in TiO_2 solution, plays a crucial rule in modifying the dielectric constant of the PTP film. The higher the TiO_2 content used in the PTP film, the higher the dielectric constant of PTP film can be obtained. However, using high TiO_2 content led to a reduction in the dielectric constant of the PTP film due to leakage current induced by the agglomeration of TiO_2. The utilization of the top-gate insulator containing TiO_2 significantly enhanced several P3HT-OFETs characteristics, e.g., an increase in the I_{on}/I_{off} ratio, and a decrease in the threshold voltage. However, the use of the PTP top-gate insulator with a high content of TiO_2 resulted in regressions in the OFETs characteristics, such as a decrease in carrier mobility and reduction in the I_{on}/I_{off} ratio. OFETs operating at the optimum conditions of the PTP gate-insulator, with PTP thickness of 225 nm and RMS roughness of 20.0 nm, provided a dielectric constant of 7.13, a threshold voltage of -8.49 V, a saturation mobility of 2.2×10^{-4} $cm^2V^{-1}s^{-1}$, I_{on}/I_{off} ratio of 37.9, and a subthreshold slope of 0.39 V/decade.

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1. Introduction

An organic field-effect transistor (OFET) is a field-effect transistor (FET) that uses organic or polymer materials as a semiconducting layer. Such transistors offer several advantages, such as high flexibility and light weight which are suitable for wearable applications. They can be fabricated large-scale via solution processability leading to low manufacturing cost [1-3]. Therefore, OFETs are frequently applied in a wide variety of products such as optoelectronics-based devices, memory devices, and mechanical and chemical sensing and monitoring devices. However, OFETs display certain inefficient electrical characteristics compared to conventional inorganic-based FETs, e.g., low saturation mobility (μ_{sat}), low on/off current (I_{on}/I_{off}) ratio, high threshold voltage (V_{th}) and low environmental stability. The above-mentioned drawbacks obstruct the use of OFETs in practical applications. Therefore, the enhancement of the electrical properties of OFETs has become an attractive research issue [4-6].

A crucial problem generally found with the utilization of OFETs is the requirement of high V_{th}. The V_{th} is defined as the minimum required voltage applied across the gate and source (V_{GS}) of OFETs to allow the current flow from drain to source (I_{DS}). The V_{th} is strongly dependent on the ability to generate the number of field-induced carriers per unit area (N_c) in the channel at the gate insulator/semiconductor interface. The approximate value of N_c is given by equation (1).

$$N_c = \frac{k\varepsilon_0}{ed} V_{GS} \tag{1}$$

where, k is a dielectric constant, ε_0 is the permittivity of a vacuum, d is a thickness of the gate insulator, and e is the charge of an electron. Higher $k\varepsilon_0$ of the gate insulator requires lower gate potential to generate sufficient carriers to fill the traps. As consequence, OFETs with high-k gate insulator can be operated at lower V_{th}. Therefore, the use of high-k material as a gate insulator is an approach to reduce the V_{th} of OFETs [7, 8].

Among the materials used as gate insulators in FETs, metal oxides (MO), e.g., TiO_2 (k = 80), Al_2O_3 (k = 8), HfO_2 (k = 25) and ZrO_2 (k = 25), are commonly used due to their high dielectric constants compared to conventional SiO_2 gate insulators (k = 3.9) [9]. However, these materials are not suitable for use in OFETs owing to their influence on local morphology and distribution of electronics states at the interface of organic semiconductors, which lead to decrease of the mobility of transistors [10]. Alternative materials used as gate insulators in OFETs, especially in top-gate structures, are polymers, e.g., poly(methyl methacrylate) (PMMA) and poly(4-vinyl phenol) (PVP). Such materials offer several advantages, i.e., low fabrication temperature (< 150°C) which can prevent the degradation of organic semiconducting layer, and less carrier traps generated at the interface between polymeric insulator and organic semiconductor. Nevertheless, the low dielectric constant that is generally observed in polymers leading to an increase of V_{th}, is a severe limitation on the use of polymers as gate insulators in OFETs. Then, the modification of the dielectric constant of polymeric gate insulators becomes a solution to achieve the utilization of polymers as gate insulators in OFETs.

Several approaches have been proposed to modify the dielectric constant of polymeric gate insulators. First, by adding high-k materials into the polymer matrix. In this approach, metal oxide nanoparticles (NPs) such as TiO_2 and SiO_2 are promising candidates. Chen *et al.* [11, 12] reported the significant increase of dielectric constant obtained from composited PVP-TiO_2 film compared to pure PVP film. Moreover, the concentration of TiO_2 in PVP is evidently correlated to the increment of dielectric constant of composited film. However, such approaches possibly encounter a problem with non-uniform distribution of MO NPs in the composite layer. Second, by using double layers composed of high-k material and polymer as gate insulators. Yang *et al.* [13, 14] reported a

drastic increase of capacitance obtained from double layers of TiO_2 and PVP films. They noted that the capacitance was directly proportional to the dielectric constant. An increase in capacitance also meant an increase in the dielectric constant. In addition, the increasing capacitance of a double layer gate insulator correlated with the thickness of the TiO_2 layer. Compared to former approaches, the use of gate insulator with stacking layers provided the opportunity to precisely control the uniformity and fine-tuning of the properties of gate insulator.

There are two configurations used to fabricate OFETs; (i) bottom gate structures, and (ii) top-gate structures. Top-gate OFETs have many advantages. For example, the gate pattern and the channel length can be precisely fabricated by conventional photolithographic processes. The gate insulator that covers the organic layer plays an important role as a protecting layer, preventing the degradation of the organic semiconducting layer by the environment. Moreover, this configuration provides a way to modify the properties of gate insulator with external factors, e.g., chemical and biological interactions, which are suitable for the use of OFETs as sensing applications. Therefore, this research work is focused on OFETs prepared with top-gate configuration.

In this work, the insertion of TiO_2 high-*k* material sandwiched between PMMA layers is proposed to enhance the dielectric constant of the gate insulator. The self-assembled monolayer (SAM) method is used to deposit TiO_2 interlayer. The effects of TiO_2 contents on the dielectric constant of the PMMA/SAM-TiO_2/PMMA (PTP) multi-layers gate insulator was investigated from metal/insulator/metal (MIM) structure. In addition, the OFET characteristics, e.g., saturation mobility, I_{on}/I_{off} ratio, and V_{th}, were characterized from the top-gate OFET using PTP gate stack insulator and poly (3-hexylthiophene-2,5-diyl) (P3HT) as the active layer.

2. Materials and Methods

2.1 Materials

P3HT, PMMA and TiO_2 NPs (P25) were purchased from Sigma-Aldrich. Analytical reagent grade (AR grade) anisole, chloroform and 1,2 dichlorobenzene were used as solvents in this work without further purification. The 100 nm-thick indium tin oxide (ITO) coated on glass slide with a sheet resistance (R_s) of 10 ohms/square was purchased from Prazisions glas & optik GmbH.

2.2 Fabrication and characterization of PMMA/SAM-TiO_2/PMMA gate insulator

The PTP multi-layered film was used as a gate dielectric of the OFETs. The dielectric properties of the PTP film were analyzed before combining with P3HT semiconducting film. The MIM structure fabricated in this work was captured as a TEM image, as shown in Figure 1(b). The MIM structure was conducted on the ITO coated glass substrate which was used as a bottom electrode. The PMMA layer was fabricated by dissolving 60 mg/ml of PMMA in anisole and spin-coated on ITO substrate using rotation speed at 5500 rpm for 2 min in a glovebox. The samples were dried at 75°C overnight in the glovebox to remove residual solvent. Next, the samples were soaked with TiO_2 NPs dispersed in deionized (DI) water with the concentrations of 10 mg/ml for 30 min to form a TiO_2 layer. After TiO_2 coating, the samples were dried in air ambient for 5 min. To increase the amount of TiO_2 NPs, the soaking of sample in 10 mg/ml of TiO_2 solution was repeated for 2, 4, 6 and 8 cycles. After drying the samples in the glovebox overnight, the top layer of PMMA film was deposited by using the same process condition as the bottom PMMA layer. Finally, PTP multi-layer gate insulator on ITO substrate was obtained. The thickness of the PTP film was measured by Dektak3030 profilometer. The crystalline formation of SAM-TiO_2 in the PTP film was investigated via x-ray diffraction (XRD) (Rigaku, TTRAX III). The 100 nm-thick top aluminum electrode with the

dimensions of 0.75x1.925 cm^2 was fabricated on the PTP structure by thermal evaporation method (Edwards 306). The capacitance and dielectric constant versus frequency profiles obtained for each PTP gate insulator with different TiO_2 NPs concentrations were measured by precision impedance analyzer (Agilent 4294a) with a constant AC voltage of 10 mV at room temperature (25°C).

2.3 Fabrication and characterization of top-gate OFETs with PMMA/SAM-TiO_2/PMMA gate insulator

A schematic diagram of top-gate OFET structure with PTP gate insulator is shown in Figure 1(a). An interdigitated pattern of 10 nm-thick chromium (Cr) and 50 nm-thick gold (Au) layers were employed as the source-drain electrode. The channel length (L) and the channel width (W) of OFET device was 20 µm and 1673 µm, respectively. The P3HT active semiconducting layer was deposited on the source-drain electrode by spin-coating a solution of 12 mg/ml P3HT dissolved in co-solvents of chloroform: 1, 2 dichlorobenzene at 1: 0.5 volume ratio at 3000 rpm for 1 min in the glovebox. Next, the PTP multi-layer gate insulator was deposited on the P3HT layer using the same protocol as described in the previous section. The content of TiO_2 NPs in PTP gate insulator was varied through the repeat of soaking samples in TiO_2 NPs solution for 2, 4, 6 and 8 cycles. The morphology of the PTP multi-layer gate insulator deposited on the P3HT active layer was characterized by atomic force microscope (AFM) (SII Instruments, SPA400). The 70 nm-thick Al film deposited by thermal evaporation was used as a top-gate electrode. Finally, the electrical characteristics of the OFETs were measured by Keithley 6430 and 2420 source meters at room temperature (25°C).

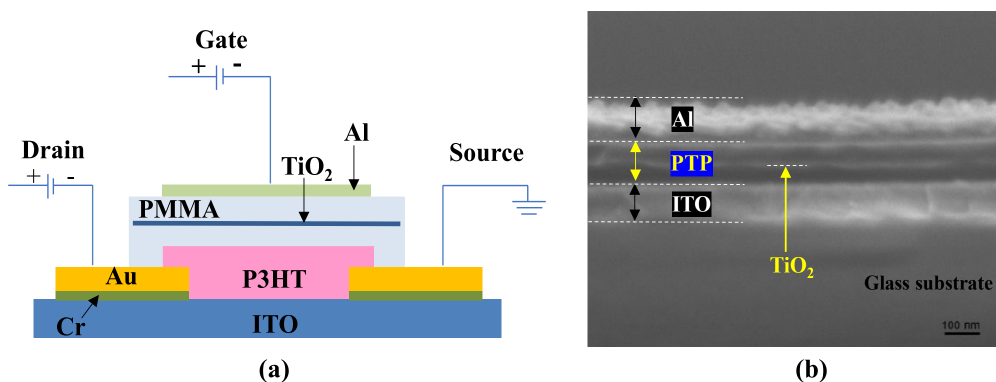
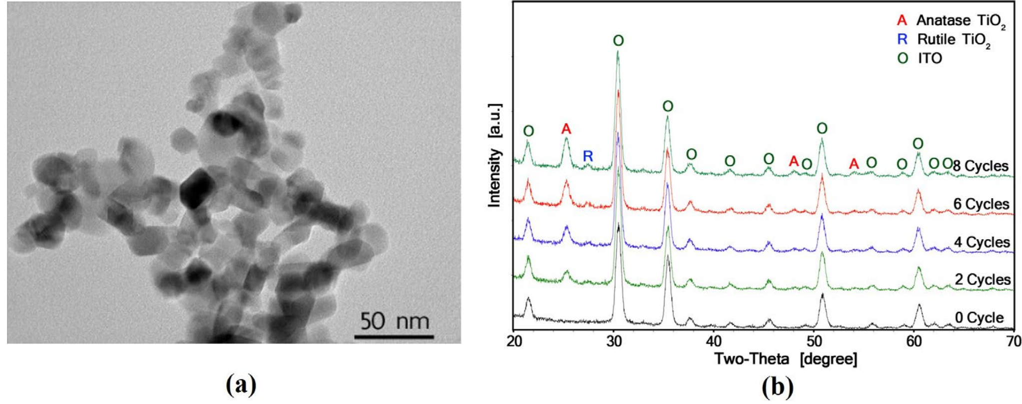


Figure 1. (a) Schematic diagram of top-gate OFETs with Al/PTP/P3HT/Au gate-stack structure and (b) cross-sectional SEM image of Al/PTP/ITO MIM structure

3. Results and Discussion

3.1 Characteristics of PMMA/TiO_2/PMMA multi-layers gate insulator

The TEM image in Figure 2(a) shows the morphology and the particle size of TiO_2 NPs which exhibited oval shape and clumped distribution with an approximately dimensional size of 18x23 nm. The X-ray diffraction (XRD) was used to characterize the PTP film coated on ITO substrate to reveal the formation of TiO_2 interlayer. The x-ray diffractograms of the PTP films obtained from different TiO_2 soaking cycles (0 to 8 cycles) are demonstrated in Figure 2(b). The diffracting peaks at 2θ angle of 25° and 28° are dominantly observed. These two peaks correspond to the diffraction



(a) **(b)**

Figure 2. (a) Transmission electron microscope (TEM) image of TiO_2 nanoparticles used in this work and (b) XRD diffractograms of PMMA/TiO_2/PMMA films prepared on ITO substrate with different soaking cycles of TiO_2

of the TiO_2 layer as anatase and rutile phases, respectively. No peak shift was observed on the x-ray diffractograms obtained from all the PTP films. This suggests that the preparation process of PTP did not affect the formation of the TiO_2 layer. Additionally, the increase in soaking cycles of sample into TiO_2 solution (up to 8 cycles) led to an increase in the intensity of diffracting peaks correlated to TiO_2. It was indicated that the more soaking cycles were applied, the higher TiO_2 content observed on PTP film.

The morphological characteristics of the PTP films prepared by different TiO_2 contents were investigated by AFM. Figures 3(a) to 3(e) illustrate the surface morphology of the PTP films with different TiO_2 soaking cycles (up to 8 cycles). The values of root mean square (RMS) surface roughness obtained from the PTP films as a function of soaking cycles are shown in Figure 3(f) and Table 1. It can be clearly observed that the surface morphology of the PTP film correlated with the content of TiO_2 existing as an interlayer. The PMMA film without TiO_2 interlayer (0 soaking cycle) exhibited smooth surface RMS roughness of 0.4 nm, with small and dense grain. With the existence of TiO_2 interlayer, the surface roughness and grain agglomeration increased. Higher number of TiO_2 soaking cycles of 8 cycles significantly increased the RMS roughness from 0.4 to 112.8 nm.

To investigate the dielectric constant of PTP multi-layers obtained from different TiO_2 contents, MIM structure using PTP as an active layer sandwiched by ITO and Al electrodes was employed. The relative dielectric constant (ε_r) was extracted through the measurement of capacitances obtained from the parallel plate capacitor using equation (2):

$$\boldsymbol{\varepsilon_r = \frac{C_i}{C_o} = \frac{\varepsilon_o \varepsilon_r A}{d C_o}} \tag{2}$$

where C_0 is the capacitance measured with a vacuum between its plates, C_i is the capacitance, A is the electrode area of the capacitor, and d is the thickness of gate insulator.

Figure 4(a) shows the capacitance-frequency (C-F) characteristics of PTP multi-layers with different TiO_2 soaking cycles. A significant enhancement of capacitance was clearly observed in the PTP films containing higher TiO_2 content. However, the capacitance was slightly decreased when the TiO_2 soaking cycles had reached 8 cycles. Since the dielectric constant was correlated to not only capacitance but also to the thickness of the dielectric layer, as shown in equation (2), the thickness of the PTP films was measured by step-profilometer. The dielectric constant-frequency

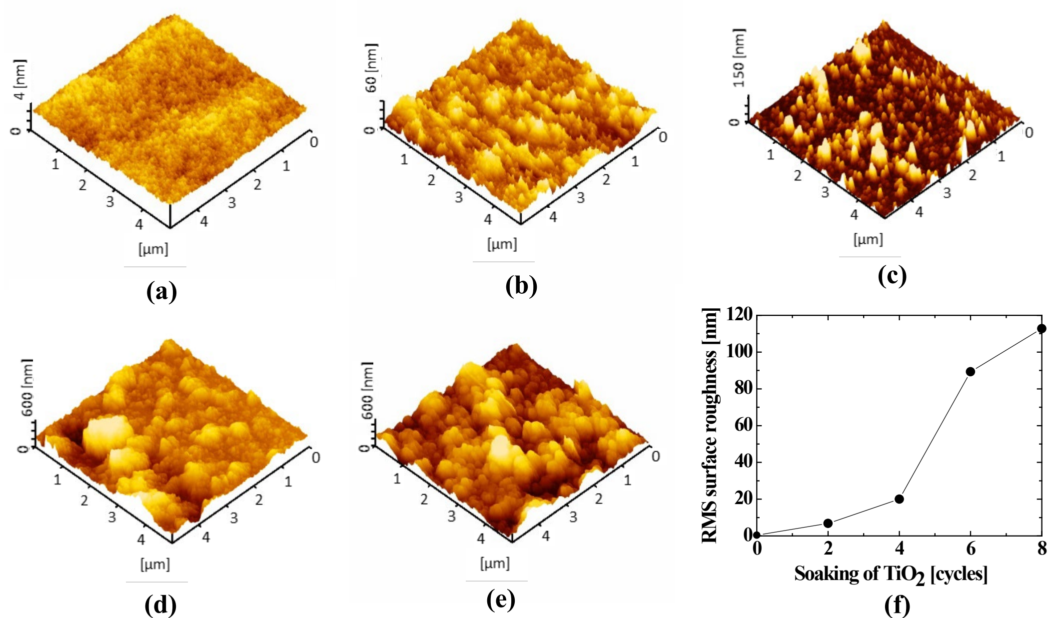


Figure 3. The AFM topographic images obtained from (a) PMMA film (without TiO_2) and PTP films prepared by (b) 2 soaking cycles, (c) 4 soaking cycles, (d) 6 soaking cycles, (e) 8 soaking cycles in TiO_2 solution, and (f) the correlation between RMS surface roughness of PTP films and TiO_2 soaking cycles

Table 1. Physical and electrical properties of the PMMA/ TiO_2/ PMMA multi-layer gate insulators with different TiO_2 soaking cycles

Soaking of TiO_2 (cycles)	C_i at 1 kHz (nF/cm^2)	Dielectric constant at 1 kHz	PTP film thickness (nm)	RMS surface roughness (nm)
0	16.5	1.78	137	0.4
2	21.3	2.74	164	6.8
4	40.3	7.13	225	20.0
6	66.8	15.7	299	89.3
8	53.8	13.2	311	112.8

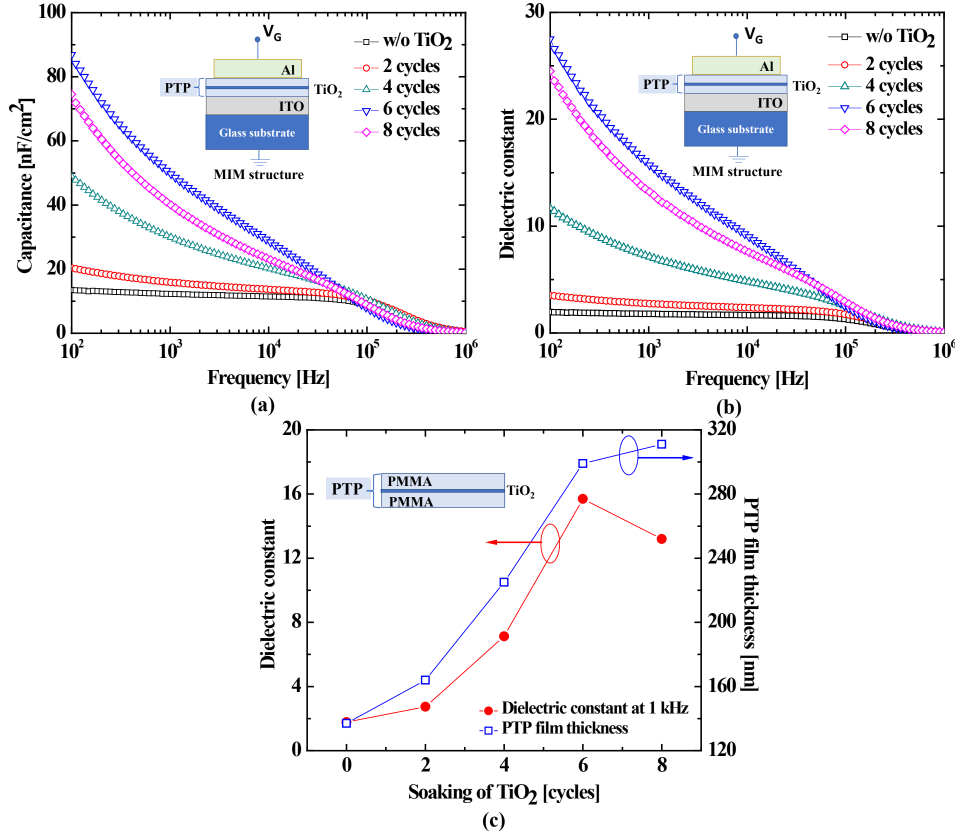


Figure 4. (a) The capacitance-frequency and (b) dielectric constant-frequency characteristics of the ITO/PMMA/TiO_2/PMMA/Al MIM capacitor prepared by varying TiO_2 soaking cycles and (c) the correlation between dielectric constant and the thickness of PTP film as a function of number of TiO_2 soaking cycles

characteristics of each PTP film were calculated using equation (2) and are illustrated in Figure 4(b). In addition, the values of capacitance and dielectric constant at the frequency of 1 kHz as well as the thicknesses of the PTP films are reported in Table 1.

Figure 4(b) shows that all PTP samples exhibited the conventional characteristic between dielectric constant versus applied frequency. The decrease of the dielectric constant at low frequency (40 Hz to 1 kHz) is attributed to the space-charge polarization of the TiO_2 interlayer [15-17]. This polarization is decreased when the dipole rotation fails to keep up with the changes in the applied electric field at higher frequency. The suppression of the dielectric constant at high frequencies (> 10^4 Hz) is caused by orientation polarization or dipole polarization. This polarization is produced by permanent electric dipoles in PMMA oriented in the direction of the applied field, which is difficult to rotate at high frequency range [18]. Then, a further decrease in the dielectric constant of the PTP films was observed at high frequency. Interestingly, the increase of the dielectric constant was clearly observed in all samples that contained TiO_2 interlayer. In comparison with the sample without TiO_2 interlayer (0 soaking cycle), the dielectric constant (at 1 kHz) of PTP multi-layer gate insulators with the soaking cycles of 2 to 6 cycles increased from 1.78 to 15.7. The correlation of dielectric constant with TiO_2 soaking cycle and the thickness of PTP films are shown in Figure 4(c). The higher the TiO_2 soaking cycles used to prepare PTP film, the higher the dielectric constant of

PTP films obtained. This result suggested that the enhancement of dielectric constant is attributed to the existence of high-*k* TiO_2 interlayer in the PTP films. However, there was a slightly decrease in dielectric constant observed in the PTP samples prepared by TiO_2 soaking cycles. The declination of dielectric constant in the PTP sample with 8 cycles soaking of TiO_2 solution is possibly explained by (i) an increase of the surface roughness and grain boundaries of PTP film that increases the interface area at a PMMA/TiO_2 interfaces [16] and (ii) the high crystallinity of TiO_2 that existed in PTP film and the surface roughness of PTP film leading to an increase in leakage current between MIM electrodes [19]. The results obtained from AFM and XRD can evidently confirm the significant increase in both surface roughness and crystallinity of the PTP sample prepared by 8 cycles of TiO_2 soaking compared to the other process conditions.

3.2 Electrical characteristics of OFETs using PMMA/TiO_2/PMMA multi-layers gate insulators

The utilization of PTP multi-layer gate insulators to enhance the characteristics of top-gate OFET devices was investigated. P3HT was employed as a semiconductor layer. The schematic structure of top-gate OFETs studied in this work is shown in Figure 1(a). The I_{DS}-V_{DS} characteristics of OFETs with different PTP films are shown in Figures 5(a)-5(e). All the OFET devices exhibited transistor characteristics, i.e. the low leakage current taking place between source-drain electrodes without the bias of gate voltage and the increase of source-drain current (I_{DS}) attributed to the increased voltage applied across the gate and source (V_{GS}). This result clearly shows that PTP film can be utilized as the gate insulator for OFETs. Moreover, the different preparation conditions of PTP film also had influence on the electrical characteristics of the constructed OFETs. With the V_{GS} at -25 V, the I_{DS} was enhanced with the increment of TiO_2 contents in the PTP gate insulator as shown in Figure 6(a). The increase of I_{DS} was likely due to the increase in the dielectric constant of the PTP films that contained thicker TiO_2 interlayer. The higher dielectric constant resulted in larger charge-carrier accumulation at the P3HT/gate insulator interface leading to the enhancement of current flow from source to drain electrodes. However, the enhancement of I_{DS} did not take place further in the OFETs using PTP gate insulators with 8 soaking cycles of TiO_2 solution. This behavior resulted from the decrease in the dielectric constant of the PTP gate insulator as shown in Table 1. This might have been caused by charge scattering at the PTP interlayer, which was due to more agglomeration of TiO_2 resulting in decreased mobility and retardation of the I_{DS} current flow. It has been noted that the slight increase in I_{DS} at V_{GS} = 0 V, observed in OFETs using PTP films with higher content of TiO_2 can possibly be attributed to the degradation of P3HT film due to exposure to moisture during the preparation of PTP gate insulator [20, 21]. During the preparation of TiO_2 interlayer, the device was directly submersed in TiO_2 aqueous solution. The water molecules possibly penetrated the PMMA layer through the P3HT. This phenomenon is clearly seen with the change of OFET characteristics when it was submersed in water for 4 h, as shown in Figure 6(b).

Figure 7(a) presents the square root of I_{DS} plotted as a function of V_{GS} for all OFET devices. From each linear fit in Figure 7(a), the threshold voltage (V_{th}) can be extracted from the x-axis intercept, and subthreshold slope (*SS*) can be extracted from Figure 7(b) using inverse slope of the I_{DS}-V_{GS} plotted. The carrier mobility (μ) is calculated from the saturation regime using the following equation [22]:

$$I_{DS} = \frac{\mu W C_i}{2L}(V_{GS} - V_{th})^2 \tag{3}$$

Where, *W* and *L* are the channel width and the channel length of OFETs, respectively. The extracted electrical parameters of the OFETs using different TiO_2 content in PTP gate insulator are summarized in Table 2.

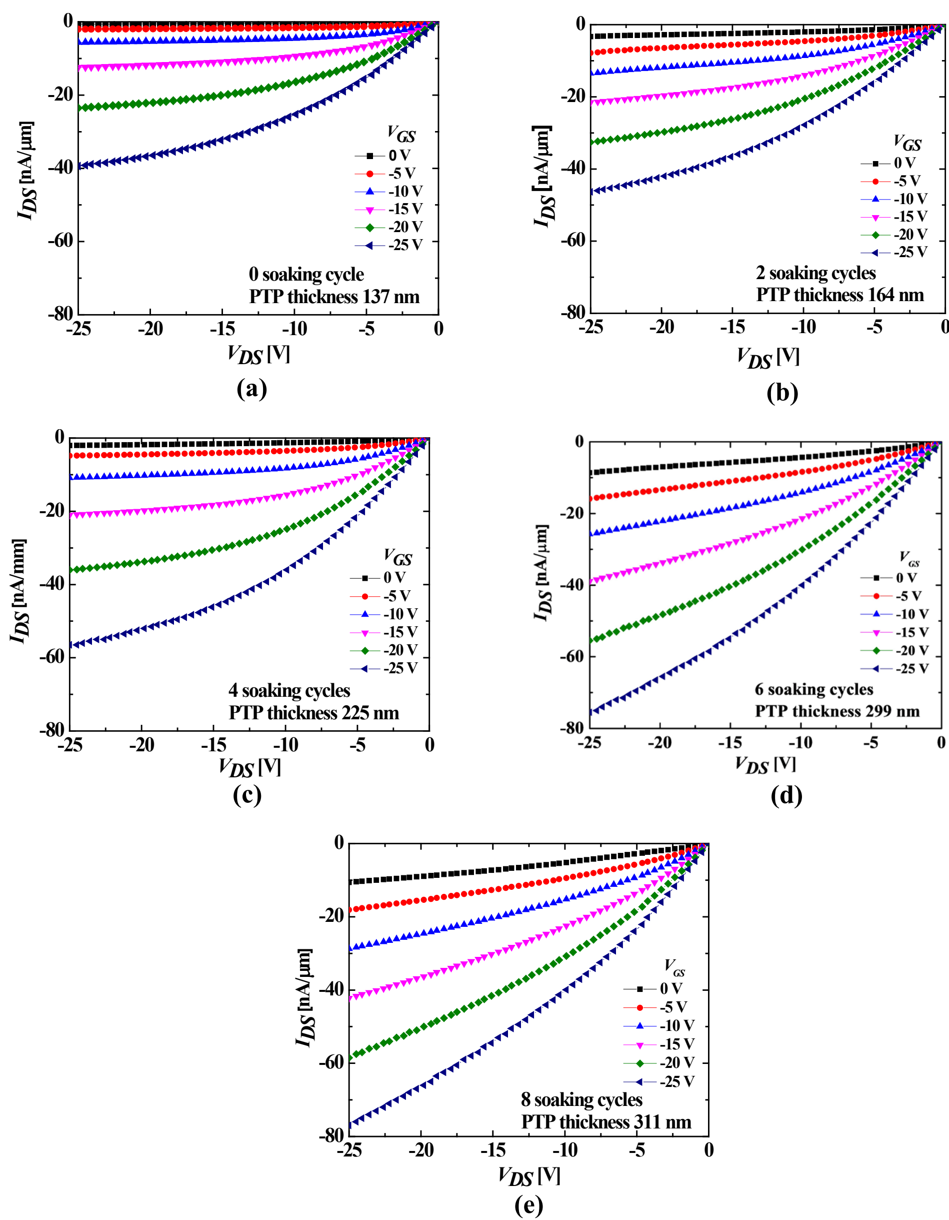


Figure 5. I_{DS}-V_{DS} characteristics of top-gated OFETs with PTP multi-layer gate insulators at the V_{GS} bias of 0 V to -25 V (a) without (w/o) TiO_2 (0 cycle) and (b) 2, (c) 4, (d) 6, and (e) 8 soaking cycles of TiO_2

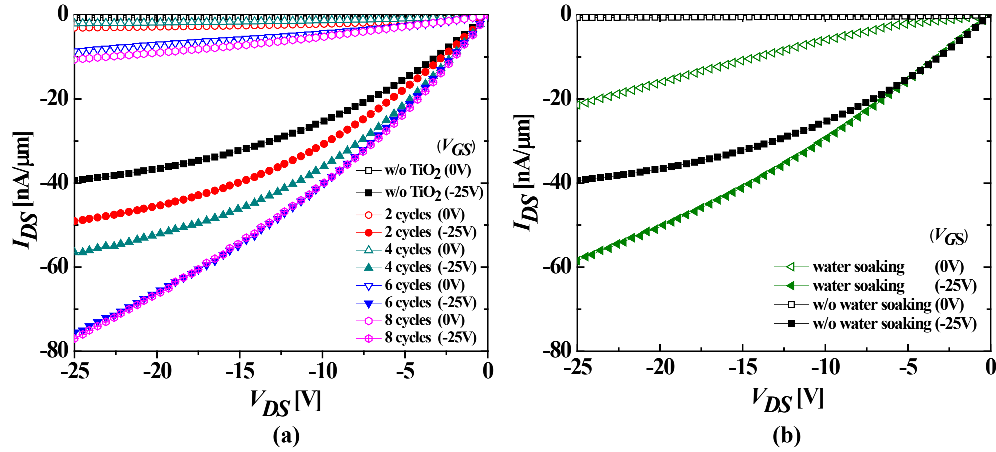


Figure 6. (a) I_{DS}-V_{DS} characteristics of top-gated OFETs with PTP multi-layer gate insulators compared at the V_{GS} bias of 0 V and -25 V at various TiO_2 soaking cycles and (b) I_{DS}-V_{DS} characteristic at V_{GS} bias of 0 V and -25 V of Al/PMMA/PMMA/P3HT/Au OFETs with and without soaking in water for 4 h

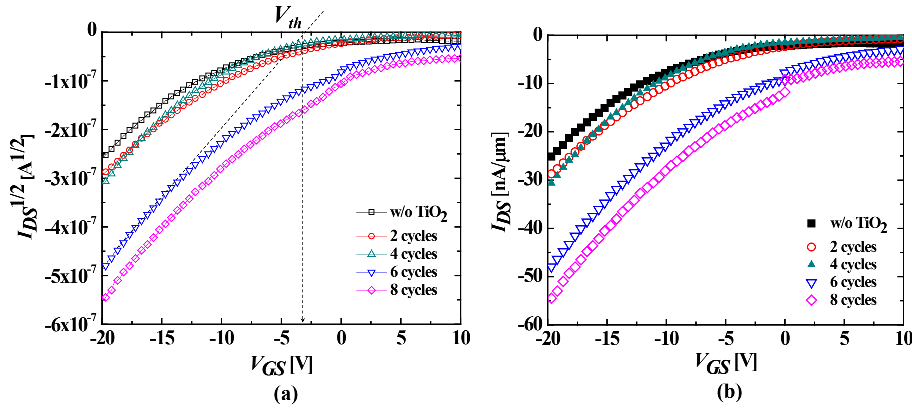


Figure 7. Transfer characteristics at the V_{DS} bias of -20 V obtained from OFETs using PTP multi-layer gate insulators with 0, 2, 4, 6 and 8 soaking cycles of TiO_2 (a) square root of I_{DS} plotted as a function of V_{GS} and (b) I_{DS} divided by gate length versus V_{GS}

Table 2. The extracted electrical parameters of top-gated OFETs using PTP multi-layer gate insulators with different TiO_2 soaking cycles

Soaking cycle of TiO_2 (cycles)	Threshold Voltage; V_{th} (V)	Saturation mobility, μ_{sat} ($cm^2V^{-1}s^{-1}$)	Subthreshold slope; *SS* (V/decade)	I_{on}/I_{off} ratio
0	-9.45	4.7 x 10^{-4}	0.49	15.6
2	-7.72	3.7 x 10^{-4}	0.49	50.4
4	-8.49	2.2 x 10^{-4}	0.40	37.9
6	-3.73	1.2 x 10^{-4}	0.39	10.7
8	-2.89	1.4 x 10^{-4}	0.38	8.5

From Table 2, the subthreshold slope (SS) is defined as $SS = dV_G/d(\log_{10}I_D)$. The SS indicates the increase of V_G required to generate one order of magnitude increase in the I_D. Typically, a low value of SS is necessary for the device operation with low voltage, high switching speed, and low power consumption. Moreover, low SS also indicate high qualities of gate insulator and interface between semiconductor and insulator. As shown in Figure 7(b) and Table 2, the OFET device without TiO_2 content in the gate dielectric (zero soaking cycle of TiO_2) exhibited a large SS of 0.49 V/decade. By using a PTP multi-layer gate insulator with the six soaking cycles of TiO_2, the SS value was significantly improved to 0.39 V/decade, which is a remarkably low number for polymer-based gate dielectric OFETs. The suppression of SS can be further improved by decreasing the thickness of the PTP multi-layer gate insulator and decreasing RMS surface roughness at the interface between semiconductor and insulator.

It was found that the I_{on}/I_{off} ratio obtained from OFETs in this work was rather low compared to that obtained from the top-gate OFETs reported in other literature. This possibly resulted from the high off-state leakage current between source and drain electrodes. Hoshino *et al.* [20] reported that the degradation of P3HT film by moisture led to the enlargement of off-state conduction of P3HT-based OFETs that operated in high moisture atmosphere. In this work, during the fabrication of PTP gate insulator, the devices were submerged in TiO_2 solution for different numbers of cycles. Therefore, the degradation of P3HT possibly took place by moisture penetrating through the PMMA layer. As the result, a high leakage current was observed. However, the I_{on}/I_{off} ratio of the OFETs increased in the devices contained higher TiO_2 content. This was likely due to the higher on-state current of the OFETs that resulted from larger accumulation of electric charges in the channel from high-k TiO_2 layer. However, at high TiO_2 soaking cycles (6 and 8 cycles), a reduction in the I_{on}/I_{off} ratio was observed although the dielectric constant of the PTP gate insulator increased. This can be explained by the deterioration of P3HT semiconducting layer during the fabrication of PTP gate insulator. To obtain high TiO_2 content in PTP films, the P3HT layer needs to be immersed in the TiO_2 solution for a longer time. The poor quality of P3HT semiconducting layer cause the increase in off-state current with respect to the on-state current of the OFETs. With the increase in the dielectric constant of PTP insulating layer containing TiO_2 contents, the charge accumulation at the channel is enhanced. Therefore, the gate voltage (V_G) needed to provide a large enough amount of charge accumulation to allow the I_{DS} to flow is reduced. The V_{th}, hence, is sequentially decreased as well.

In general, the OFETs studied in the past were bottom-gate structure, where an organic semiconductor was fabricated on top of the dielectric layer. The decrease in mobility corresponded to the increase in surface roughness of the TiO_2 NPs-embedded dielectric layer. However, such mobility degradation depending on the morphology of gate insulator did not occur with the top-gate structure employed in this research since the dielectric layer was fabricated on an organic semiconductor layer. However, there was a slight decrease in mobility observed in the top-gate OFETs using PTP gate insulators with high TiO_2 contents. This was possibly attributable to the non-uniform local charge accumulation induced by the PTP gate insulator with high content of TiO_2. The agglomeration of TiO_2 that occurred resulted in high surface roughness as well as increase of grain boundary at the interface of PMMA and TiO_2, which reduced the amorphous nature of TiO_2 gate insulator. This can cause a reduction of the carrier mobility due to the interface trapped charges, electrons or holes, which are trapped at the semiconductor and insulator interface [23]. Moreover, the agglomeration of TiO_2 can cause thickness variation in the PTP film which may lead to leakage current in the device, and then an unstable of I_{on}/I_{off} ratio is observed with increase of TiO_2 content. The AFM micrographs in Figure 3 show that high TiO_2 content in PTP films leads to increment in surface roughness. The rough surface of the PTP originated from the agglomeration of TiO_2 NPs into large clusters. Therefore, the distribution of local dielectric constant at each domain in the PTP gate insulator is non-uniform. As a consequence, the local charge accumulation at each domain in the conductive channel is also non uniform. As result, the reduction in channel uniformity leads to

an increase in resistance in the conducting channel. Then, lower charge mobility takes place in the OFETs. The performance of PMMA/TiO_2/PMMA (PTP) multi-layer gate insulators compared to the bottom-gate OFETs from others who reported high-*k* gate insulators is shown in Figure 8. Although the PTP multi-layer gate insulators from this work provided low mobility, a high dielectric constant compared to that of other works was obtained. The OFETs behavior was also obtained by using a PTP gate stack insulator which suggested an alternative way for easy and fast fabrication of high-*k* -PMMA hybrid material. However, the total thickness of the PTP multi-layer gate insulator and the TiO_2 content should be further investigated to reduce the surface roughness at the semiconductor and insulator interface to improve carrier mobility.

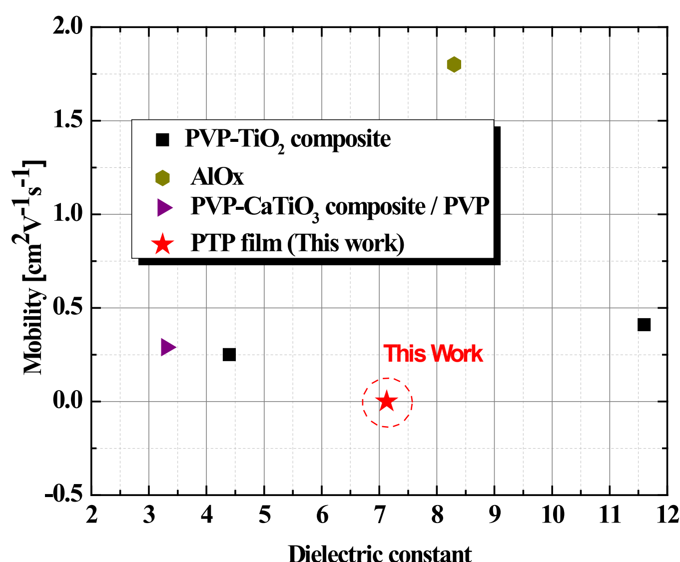


Figure 8. Comparison of the performance of top-gate OFETs with PTP multi-layer gate insulator and the bottom-gate OFETs from other research work

4. Conclusions

The utilization of PMMA/TiO_2/PMMA (PTP) multi-layers as an alternative high-*k* gate insulator for top-gate P3HT-based OFETs film was proposed. The TiO_2 content of the PTP film played a key role in modifying the dielectric constant of the gate insulator. When the optimum content of TiO_2 in the PTP film was used, a high dielectric constant of PTP film was obtained. However, the use of high TiO_2 content and conducting phase led to decrease of the dielectric constant due to leakage current. By applying the PTP film as top-gate insulator, the OFET characteristics were improved, e.g., an increase in I_{on}/I_{off} ratio and a decrease in threshold voltage were seen. The enhancement of OFET characteristics was attributed to the better induction of charge accumulation by the PTP film containing TiO_2 interlayer. However, the degradations in OFET performance, e.g., the reduction in I_{on}/I_{off} ratio and the slight decrease in mobility were observed in devices that used PTP gate insulators with high TiO_2 contents. The degradation of OFET characteristics corresponded to (i) the deterioration of P3HT by moisture during the fabrication of the PTP gate insulator and (ii) the non-uniform local charge accumulation that resulted from the agglomeration of TiO_2 in the PTP gate insulator.

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